HITACHI

No. 0155

HTD-K180UK
HTD-K180E

SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:

Before servicing this chassis, it is important that the service technician read the “Safety Precautions” and “Product Safety Notices” in this service manual.

ATTENTION:

Avant d’effectuer l’entretien du châassis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise“ und „Hinweise zur Produktsicherheit“ in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d’entretien peuvent faire l’objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

Home Cinema
October 2004

1. GENERAL DESCRIPTION

1.1 MT 1379

The MT1370 Progressive Scan DVD Player Combo chip is a single-chip MPEG video decoding chip that integrates audio/video stream data processing, TV encoder four video DACs with macrovision, copy protection, DVD system navigation, system control and housekeeping functions.
These features can be listed as follows:

General Features:

- Progressive scan DVD-player combo chip.

- Support NTSC, PAL-BDGHI, PAL-N, PAL-M interlace TV format and 480p, 576p progressive TV format.

- Built-in progressive video output.

- DVD-Video, VCD 1.1, 2.0 and SVCD.

- Unified track buffer A/V decoding buffer.

- Supports 16-bit/32-bit SDRAM data bus interface.

- Servo controlling and data channel processing.

Video Related Features:

· Macrovision 7.1 for NTSC/PAL interlaced video.

· Simultaneous composite video and S-video outputs, or composite and YUV outputs, or composite and RGB outputs.

· 8-bit CCIR 601 YUV 4:2:2 output.

. Decodes MPEG video and MPEG2 main profile at main level.

· Maximum input bit rate of 15 Mbits/sec.

Audio Related Features:

· Dolby Digital (AC-3) and Dolby Pro Logic.

· Dolby Digital S/PDIF digital oudio outputs.

· High-Definition Compatible Digital (HDCD) decoding.

· CD-DA.

· MP3.

1.2 MEMORY

SDRAM Memory Interface

The MT1379 provides a glueless a 16-bit interface to DRAM memory devices used as OSD MPEG stream and video buffer memory for a DVD player. The maximum amount of memory supported is 16 Mb of Synchronous DRAM (SDRAM). The memory interface is configurable in depth to support 128 Mb adressing. The memory

interface controls access to both external SDRAM memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

1.3 DRIVE INTERFACES

The MT1379 supports the DV34 interface, and other RF and servo interfaces used by any types of DVD loaders. These interfaces meet the specifications of many DVD loader manufacturers.

1.4 FRONT PANEL

The front panel is based around an Futaba VFD and a common NEC front panel controller chip, (uPD16311). The MT1379 controls the uPD16311 using several control signals, (clock, data, chip select). The infrared remote control signal is passed directly to the MT1379 for decoding.

1.5 REAR PANEL

A typical rear panel is included in the referance design. This rear panel supports:

- Six channel or two channel audio outputs.

- Optical and coax S/PDIF outputs.

- Composite, S-Video, and SCART outputs.

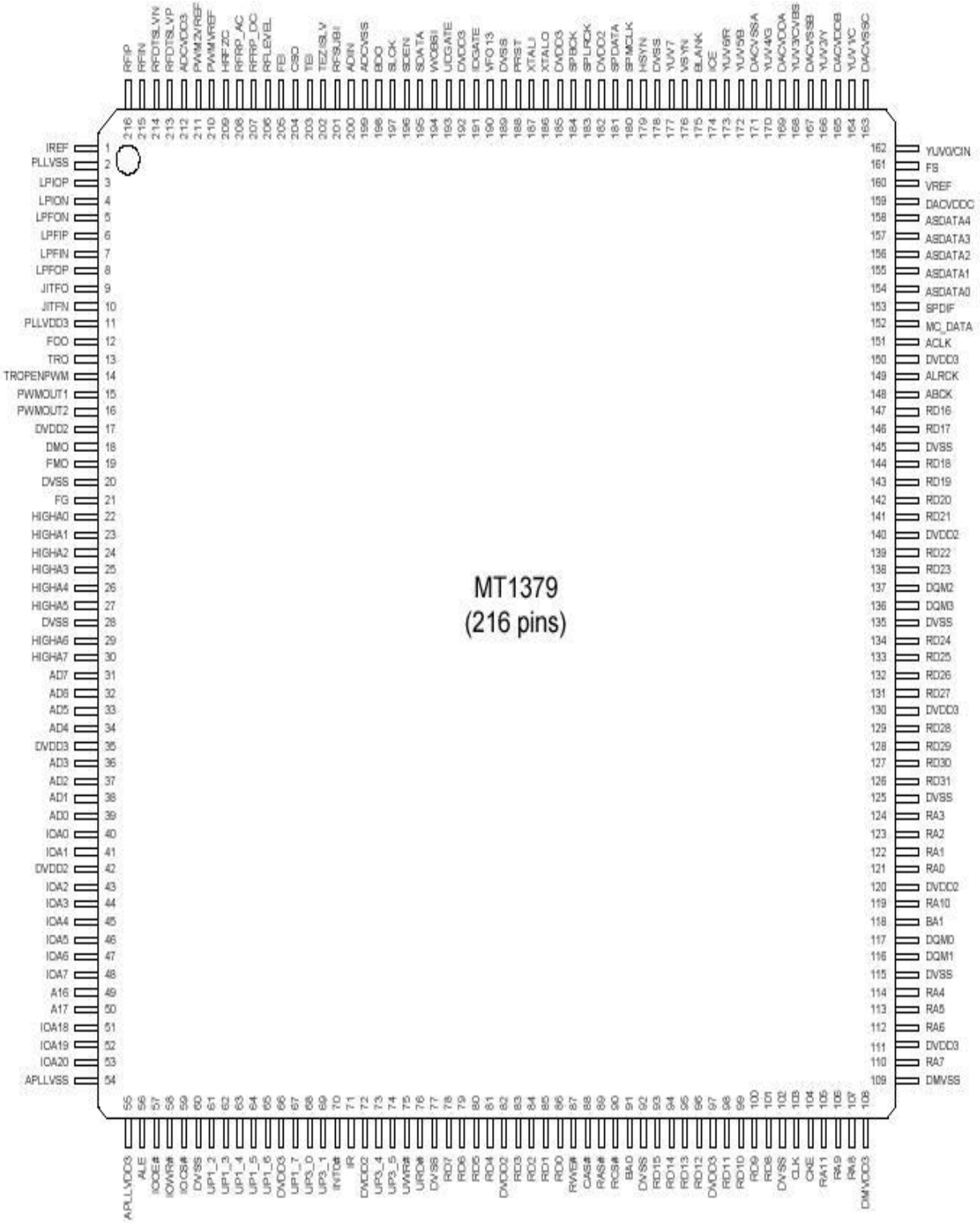
The six-video signals used to provide CVBS, S-Video, and RGB are generated by the MT1379's internal video DAC. The video signals are buffered by external circutiry.

The S/PDIF serial stream is also generated by the MT1379 output by the rear panel. AK4382, CS4392 Audio DACs are used for two channel audio output with MT1379.

12-pin DDX board output jack gives out the amplified audio. Digital Audio is processed in the DDX-8228 IC and then amplified in the DDX-2050 Power Amplifier ICs.

2. SYSTEM BLOCK DIAGRAM and MT1379 PIN DESCRIPTION

2.1 MT1379 PIN DESCRIPTION



Pin Number	Symbol	Type	Description
1	IREF	Analog Input	Current reference input. It generates reference current for data PLL. Connect an external 100K resistor to this pin and PLLVSS.
2	PLLVSS	Ground	Ground pin for data PLL and related analog circuitry
3	LPIOP	Analog Output	Positive output of the low pass filter
4	LPION	Analog Output	Negative output of the low pass filter
5	LPFON	Analog output	Negative output of loop filter amplifier
6	LPFIP	Analog Input	Positive input of loop filter amplifier
7	LPFIN	Analog Input	Negative input of loop filter amplifier
8	LPFOP	Analog Output	Positive output of loop filter amplifier
9	JITFO	Analog Output	RF jitter meter output
10	JITFN	Analog Input	Negative input of the operation amplifier for RF jigger meter
11	PLLVDD3	Power	3.3V power pin for data PLL and related analog circuitry
12	FOO	Analog Output	Focus servo output. PDM output of focus servo compensator
13	TRO	Analog Output	Tracking servo output. PDM output of tracking servo compensator
14	TROPENPWM	Analog Output	Tray open output, controlled by microcontroller. This is PWM output for TRWMEN27hRW2=1 or is digital output for TRWMEN27hRW2=0
15	PWMOUT1	Analog Output	The 1st general PWM output
16	PWMOUT2	Analog Output	The 2nd general PWM output
17	DVDD2	Power	2.5V power pin for internal fully digital circuitry
18	DMO	Analog Output	Disk motor control output. PWM output
19	FMO	Analog Output	Feed motor control. PWM output
20	DVSS	Ground	Ground pin for internal fully digital circuitry
21	FG	Input	Motor Hall sensor input
22	HIGHA0	Inout 2~16MA, SR PU	Microcontroller address 8
23	HIGHA1	Inout 2~16MA, SR PU	Microcontroller address 9
24	HIGHA2	Inout 2~16MA, SR PU	Microcontroller address 10
25	HIGHA3	Inout 2~16MA, SR PU	Microcontroller address 11
26	HIGHA4	Inout 2~16MA, SR PU	Microcontroller address 12
27	HIGHA5	Inout 2~16MA, SR PU	Microcontroller address 13
28	DVSS	Ground	Ground pin for internal digital circuitry
29	HIGHA6	Inout 2~16MA, SR PU	Microcontroller address 14

Pin Number	Symbol	Type	Description
30	HIGHA7	Inout 2~16MA, SR PU	Microcontroller address 15
31	AD7	Inout 2~16MA, SR	Microcontroller address/data 7
32	AD6	Inout 2~16MA, SR	Microcontroller address/data 6
33	AD5	Inout 2~16MA, SR	Microcontroller address/data 5
34	AD4	Inout 2~16MA, SR	Microcontroller address/data 4
35	DVDD3	Power	3.3V power pin for internal digital circuitry
36	AD3	Inout 2~16MA, SR	Microcontroller address/data 3
37	AD2	Inout 2~16MA, SR	Microcontroller address/data 2
38	AD1	Inout 2~16MA, SR	Microcontroller address/data 1
39	AD0	Inout 2~16MA, SR	Microcontroller address/data 0
40	IOA0	Inout 2~16MA, SR PU	Microcontroller address 0 / IO
41	IOA1	Inout 2~16MA, SR PU	Microcontroller address 1 / IO
42	DVDD2	Power	2.5V power pin for internal digital circuitry
43	IOA2	Inout 2~16MA, SR PU	Microcontroller address 2 / IO
44	IOA3	Inout 2~16MA, SR PU	Microcontroller address 3 / IO
45	IOA4	Inout 2~16MA, SR PU	Microcontroller address 4 / IO
46	IOA5	Inout 2~16MA, SR PU	Microcontroller address 5 / IO
47	IOA6	Inout 2~16MA, SR PU	Microcontroller address 6 / IO
48	IOA7	Inout 2~16MA, SR PU	Microcontroller address 7 / IO
49	A16	Output 2~16MA, SR	Flash address 16
50	A17	Output 2~16MA, SR	Flash address 17

Pin Number	Symbol	Type	Description
51	IOA18	Inout 2~16MA, SR SMT	Flash address 18 / IO
52	IOA19	Inout 2~16MA, SR SMT	Flash address 19 / IO
53	IOA20	Inout 2~16MA, SR SMT	Flash address 20 / IO OR Videoin Data PortB 0
54	APLLVSS	Ground	Ground pin for audio clock circuitry
55	APLLVDD3	Power	3.3V Power pin for audio clock circuitry
56	ALE	Inout 2~16MA, SR PU, SMT	Microcontroller address latch enable
57	IOOE#	Inout 2~16MA, SR SMT	Flash output enable, active low / IO
58	IOWR#	Inout 2~16MA, SR SMT	Flash write enable, active low / IO
59	IOCS#	Inout 2~16MA, SR PU, SMT	Flash chip select, active low / IO
60 61	DVSS UP1_2	Ground Inout 4MA, SR PU, SMT	Ground pin for internal digital circuitry Microcontroller port 1-2
62	UP1_3	Inout 4MA, SR PU, SMT	Microcontroller port 1-3
63	UP1_4	Inout 4MA, SR PU, SMT	Microcontroller port 1-4
64	UP1_5	Inout 4MA, SR PU, SMT	Microcontroller port 1-5
65	UP1_6	Inout 4MA, SR PU, SMT	Microcontroller port 1-6
66	DVDD3	Power	3.3V power pin for internal digital circuitry
67	UP1_7	Inout 4MA, SR PU, SMT	Microcontroller port 1-7
68	UP3_0	Inout 4MA, SR PU, SMT	Microcontroller port 3-0
69	UP3_1	Inout 4MA, SR PU, SMT	Microcontroller port 3-1

Pin Number	Symbol	Type	Description
70	INT0#	Inout 2~16MA, SR PU, SMT	Microcontroller interrupt 0, active low
71	IR	Input SMT	IR control signal input
72	DVDD2	Power	2.5V power pin for internal digital circuitry
73	UP3_4	Inout	Microcontroller port 3-4
74	UP3_5	Inout	Microcontroller port 3-5
75	UWR#	Inout 2~16MA, SR PU, SMT	Microcontroller write strobe, active low
76	URD#	Inout 2~16MA, SR PU, SMT	Microcontroller read strobe, active low
77	DVSS	Ground	Ground pin for internal digital circuitry
78	RD7	Inout	DRAM data 7
79	RD6	Inout	DRAM data 6
80	RD5	Inout	DRAM data 5
81	RD4	Inout	DRAM data 4
82	DVDD2	Power	2.5V power pin for internal digital circuitry
83	RD3	Inout	DRAM data 3
84	RD2	Inout	DRAM data 2
85	RD1	Inout	DRAM data 1
86	RD0	Inout	DRAM data 0
87	RWE#	Output 2~16MA, SR	DRAM Write enable, active low
88	CAS#	Output 2~16MA, SR	DRAM columnaddress strobe, active low
89	RAS#	Output 2~16MA, SR	DRAM row address strobe, active low
90	RCS#	Output 2~16MA, SR	DRAM chip select, active low
91	BA0	Output 2~16MA, SR	DRAM bank address 0
92	DVSS	Ground	Ground pin for internal digital circuitry
93	RD15	Inout 2~16MA, SR PU/PD, SMT	DRAM data 15
94	RD14	Inout 2~16MA, SR PU/PD, SMT	DRAM data 14
95	RD13	Inout 2~16MA, SR PU/PD, SMT	DRAM data 13
96	RD12	Inout 2~16MA, SR PU/PD, SMT	DRAM data 12
97	DVDD3	Power	3.3V power pin for internal digital circuitry

Pin Number	Symbol	Type	Description
98	RD11	Inout 2~16MA, SR PU/PD, SMT	DRAM data 11
99	RD10	Inout 2~16MA, SR PU/PD, SMT	DRAM data 10
100	RD9	Inout 2~16MA, SR PU/PD, SMT	DRAM data 9
101	RD8	Inout 2~16MA, SR PU/PD, SMT	DRAM data 8
102	DVSS	Ground	Ground pin for internal digital circuitry
103	CLK	Output 2~16MA, SR	DRAM clock
104	CLE	Output 2~16MA, SR	DRAM clock enable
105	RA11	Output 2~16MA, SR	DRAM address bit 11 or audio serial data 3 (channel 7/8)
106	RA9	Output 2~16MA, SR	DRAM address 9
107	RA8	Output 2~16MA, SR	DRAM address 8
108	DMVDD3	Power	3.3V Power pin for DRAM clock circuitry
109	DMVSS	Ground	Ground pin for DRAM clock circuitry
110	RA7	Output 2~16MA, SR	DRAM address 7
111	DVDD3	Power	
112	RA6	Output 2~16MA, SR	DRAM address 6
113	RA5	Output 2~16MA, SR	DRAM address 5
114	RA4	Output 2~16MA, SR	DRAM address 4
115	DVSS	Ground	Ground pin for internal digital circuitry
116	DQM1	Output 2~16MA, SR	Mask for DRAM input/output byte 1
117	DQM0	Output 2~16MA, SR	Mask for DRAM input/output byte 0
118	BA1	Output 2~16MA, SR	DRAM bank address 0
119	RA10	Output 2~16MA, SR	DRAM address10
120	DVDD2	Power	2.5V power pin for internal digital circuitry
121	RA0	Output 2~16MA, SR	DRAM address 0
122	RA1	Output 2~16MA, SR	DRAM address 1

Pin Number	Symbol	Type	Description
123	RA2	Output 2~16MA, SR	DRAM address 2
124	RA3	Output 2~16MA, SR	DRAM address 3
125	DVSS	Ground	Ground pin for internal digital circuitry
126	RD31	Inout 2~16MA, SR PU/PD, SMT	DRAM data 31
127	RD30	Inout 2~16MA, SR PU/PD, SMT	DRAM data 30
128	RD29	Inout 2~16MA, SR PU/PD, SMT	DRAM data 29
129	RD28	Inout 2~16MA, SR PU/PD, SMT	DRAM data 28
130	DVDD3	Power	3.3V power pin for internal digital circuitry
131	RD27	Inout 2~16MA, SR PU/PD, SMT	DRAM data 27
132	RD26	Inout 2~16MA, SR PU/PD, SMT	DRAM data 26
133	RD25	Inout 2~16MA, SR PU/PD, SMT	DRAM data 25
134	RD24	Inout 2~16MA, SR PU/PD, SMT	DRAM data 24
135	DVSS	Ground	Ground pin for internal digital circuitry
136	DQM3	Output 2~16MA, SR	Mask for DRAM input/output byte 3
137	DQM2	Output 2~16MA, SR	Mask for DRAM input/output byte 2
138	RD23	Inout 2~16MA, SR PU/PD, SMT	DRAM data 23 / Videoin Data PortA 7
139	RD22	Inout 2~16MA, SR PU/PD, SMT	DRAM data 22 / Videoin Data PortA 6
140	DVDD2	Power	2.5V power pin for internal digital circuitry
141	RD21	Inout 2~16MA, SR PU/PD, SMT	DRAM data 21 / Videoin Data PortA 5
142	RD20	Inout 2~16MA, SR PU/PD, SMT	DRAM data 20 / Videoin Data PortA 4

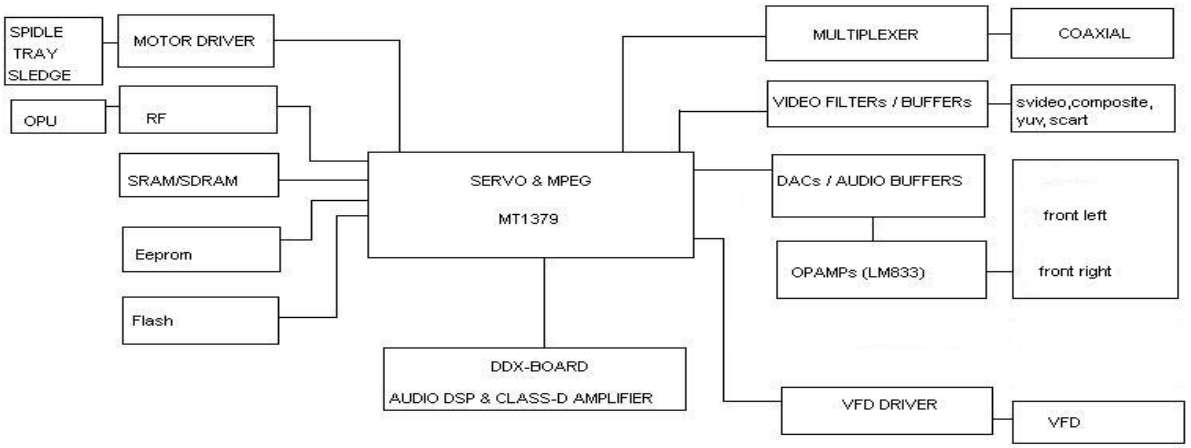
Pin Number	Symbol	Type	Description
143	RD19	Inout 2~16MA, SR PU/PD, SMT	DRAM data 19 / Videoin Data PortA 3
144	RD18	Inout 2~16MA, SR PU/PD, SMT	DRAM data 18 / Videoin Data PortA 2
145	DVSS	Ground	Ground pin for internal digital circuitry
146	RD17	Inout 2~16MA, SR PU/PD, SMT	DRAM data 17 / Videoin Data PortA 1
147	RD16	Inout 2~16MA, SR PU/PD, SMT	DRAM data 16 / Videoin Data PortA 0
148	ABCK	Output 4MA	Audio bit clock
149	ALRCK	Inout 4MA, PD, SMT	(1) Audio left/right channel clock (2) Trap value in power-on reset : 1 : use external 373 0: use internal 373
150	DVDD3	Power	3.3V power pin for internal digital circuitry
151	ACLK	Inout 4MA	Audio DAC master clock (384/256 audio sample frequency)
152	MC_DATA	Input	Microphone serial input
153	SPDIF	Output 2~16MA, SR : ON/OFF	SPDIF output
154	ASDATA0	Inout 4MA PD SMT	(1) Audio serial data 0 (left/right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
155	ASDATA1	Inout 4MA PD SMT	(1) Audio serial data 1 (surround left/surround right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
156	ASDATA2	Inout 4MA PD SMT	(1) Audio serial data 2 (center/left channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
157	ASDATA3	Inout 4MA PD SMT	(1) Audio serial data 3 (surround left/surround right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation OR Videoin Data PortB 1
158	ASDATA4	Inout 4MA PD SMT	(1) Audio serial data 4 (center/left channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation OR Videoin Data PortB 2
159	DACVDDC	Power	3.3V power pin for VIDEO DAC circuitry
160	VREF	Analog input	Bandgap reference voltage
161	FS	Analog output	Full scale adjustment
162	YUV0/CIN	Output 4MA, SR	Video data output bit 0 / Compensation capacitor
163	DACVSSC	Ground	Ground pin for VIDEO DAC circuitry

Pin Number	Symbol	Type	Description
164	YUV1/C	Output 4MA, SR	Video data output bit 1 / Analog chroma output
165	DACVDDB	Power	3.3V power pin for VIDEO DAC circuitry
166	YUV2/Y	Output 4MA, SR	Video data output bit 2 / Analog Y output
167	DACVSSB	Ground	Ground pin for VIDEO DAC circuitry
168	YUV3/CVBS	Output 4MA, SR	Video data output bit 3 / Analog composite output
169	DACVDDA	Power	3.3V power pin for VIDEO DAC circuitry
170	YUV4/G	Output 4MA, SR	Video data output bit 4 / Green or Y
171	DACVSSA	Ground	Ground pin for VIDEO DAC circuitry
172	YUV5/B	Output 4MA, SR	Video data output bit 5 / Blue or CB
173	YUV6/R	Output 4MA, SR	Video data output bit 6 / Red or CR
174	ICE	Input PD, SMT	Microcontroller ICE mode enable
175	BLANK#	Inout 4MA, SR SMT	Video blank area, active low / Videoin Field_601
176	VSYN	Inout 4MA, SR SMT	Vertical sync / Videoin Vsync_601
177	YUV7	Inout 4MA, SR SMT	Video data output bit 7 / Videoin Data PortB 3
178	DVSS	Ground	Ground pin for internal digital circuitry
179	HSYN	Inout 4MA, SR SMT	Horizontal sync / Videoin Hsync_601
180	SPMCLK	Input	Audio DAC master clock of SPDIF input / Videoin Data PortB 4
181	SPDATA	Input	Audio data of SPDIF input / Videoin Data PortB 5
182	DVDD2	Power	2.5V power pin for internal digital circuitry
183	SPLRCK	Input	Audio left/right channel clock of SPDIF input / Videoin Data PortB 6
184	SPBCK	Input	Audio bit clock of SPDIF input / Videoin Data PortB 7
185	DVDD3	Power	3.3V power pin for internal digital circuitry
186	XTALO	Output	Crystal output
187	XTALI	Input	Crystal input
188	PRST	Input PD, SMT	Power on reset input, active high
189	DVSS	Ground	Ground pin for internal digital circuitry
190	VFO13	Output	The 1st, 3rd header VFO pulse output
191	IDGATE	Output	Header detect signal output
192	DVDD3	Power	3.3V power pin for internal digital circuitry

Pin Number	Symbol	Type	Description
193	UDGATE	Output	DVD_RAM recording data gate signal output
194	WOBSI	Input	Wobble signal input
195	SDATA	Output	RF serial data output
196	SDEN	Output	RF serial data latch enable
197	SLCK	Output	RF serial clock output
198	BDO	Input	Flag of defect data input status
199	ADCVSS	Ground	Ground pin for ADC circuitry
200	ADIN	Analog Input	General A/D input
201	RFSUBI	Analog Input	RF subtraction signal input terminal
202	TEZISLV	Analog Input	Tracking error zero crossing low pass input
203	TEI	Analog Input	Tracking error input
204	CSO	Analog Input	Central servo input
205	FEI	Analog Input	Focus error input
206	RFLEVEL	Analog Input	Sub beam add input or RFRP low pass input
207	RFRP_DC	A Input	RF ripple detect input
208	RFRP_AC	Analog Input	RF ripple detect input (through AC coupling)
209	HRFZC	Analog Input	High frequency RF ripple zero crossing
210	PWMVREF	A Input	A reference voltage input for PWM circuitry. A typical value of 4.0 v
211	PWM2VREF	A Input	A reference voltage input for PWM circuitry. A typical value of 2.0 v
212	ADCVDD3	Power	3.3V power pin for ADC circuitry
213	RFDTSLVP	Analog Output	Positive RF data slicer level output
214	RFDTSLVN	Analog Output	Negative RF data slicer level output
215	RFIN	Analog Input	Negative input of RF differential signal
216	RFIP	Analog Input	Positive input of RF differential signal

2.1 SYSTEM BLOCK DIAGRAM

System block diagram is shown in the following figure:



3. AUDIO OUTPUT

The MT1379 supports the stereo (2 channel) outputs .

The MT1379 alTrso provides digital output in S/PDIF format. The board supports coaxial S/PDIF input.

AV2300 has also 5.1 channel Class-D amplifier outputs to 8 ohms satelites and 4 ohms subwoofer.

4 AUDIO DACS

The MT1379 supports several variations of an I 2 S type bus, varying the order of the data bits (leading or no leading zero bit, left or right alignment within frame, and MSB or LSB first) is possible using the MT1379 internal configuration registers. The I 2 S format uses four stereo data lines and three clock lines. The I 2 S data and clock lines can be connected directly to one or more audio DAC to generate analog audio output.

The two-channel DAC is an AKM AK4382 . The DACs support up to 192kHz sampling rate.

The outputs of the DACs are differential, not single ended so a buffering circuit is required. The buffer circuits use National LM833 op-amps to perform the low-pass filtering and the buffering.

5 VIDEO INTERFACE

5.1 Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the Vibratto. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode.

The video output section features internal line buffers which allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV4: 2:2 to YUV4: 2:0 component and sample conversion. A polyphase filter achieves arbitrary horizontal decimation and interpolation.

Video Bus

The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

Video Post-Processing

The MT1379 video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

Video Timing

The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays.

6 FLASH MEMORY

The decoder board supports AMD class Flash memories. Currently 4 configurations are supported:

FLASH_512K_8b
FLASH_1024K_8b
FLASH_512Kx2_8b
FLASH_512Kx2_16b

The Vibratto permits both 8- and 16-bit common memory I/O accesses with a removable storage card via the host interface.

7 SERIAL EEPROM MEMORY

An I2C serial EEPROM is used to store user configuration (i.e. language preferences, speaker setup, etc.) and software configuration.. Industry standard EEPROM range in size from 1kbit to 256kbit and share the same IC footprint and pinout. The default device is 2kbit, 256kx 8, SOIC8 SGS Thomson ST24C02M1 or equivalent.

8 AUDIO INTERFACE AUDIO SAMPLING RATE AND PLL COMPONENT CONFIGURATION

The MT1379 audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard I^2S interface input and output and S/PDIF (IEC958) audio output. Stereo mode is in I^2S format while six channels Dolby Digital (5.1 channel) audio output can be channeled through the S/PDIF. The S/PDIF interface consists of a bi-phase mark encoder, which has low skew. The transmit I^2S interface supports the 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz. The audio samples for the I^2S transmit interface can be 16, 18, 20, 24, and 32-bit samples.

For Linear PCM audio stream format, the MT1379 supports 48 kHz and 96 kHz. Dolby Digital audio only supports 48 kHz. MT1379 incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock. The MCLK pin is for the audio DAC clock and can either be an output from or an input to the MT1379. Audio data out (TSD) and audio frame sync (TWS) are clocked out of the MT1379 based on the audio transmit bit clock (TBCK). Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS).

9 FRONT PANEL

9.1 VFD CONTROLLER

The VFD controller is a NEC uPD16311. This controller is not a processor, but doesinclude a simple state machine which scans the VFD and reads the front panel button matrix. The 16311 also includes RAM so it can store the current state of all the VFD icons and segments. Therefore, the 16311 need only be accessed when the VFD status changes and when the button status is read. The MT1379 can control this chip by using 3 wire communication.

10 CONNECTORS

10.1 SCART CONNECTORS

Pinout of the scart connector:
1 - Audio Right Out
2 - Audio Right In
3 - Audio Left / Mono Out
4 - Audio Gnd
5 - Blue Gnd

6 - Audio Left / Mono In
7 - Blue
8 - Control Voltage
9 - Green Gnd
10 - Comms Data 2
11 - Green
12 - Comms Data 1
13 - Red Gnd
14 - Comms Data Gnd
15 - Red
16 - Fast Blanking
17 - Video Gnd
18 - Fast Blanking Gnd
19 - Composite Video In
20 - Composite Video Out
21 – Shield Gnd

Some cheaper SCART cables use unshielded wires, which is just about acceptable for short cable lengths. For longer lengths, shielded co-ax cable become essential.

Scart Signals:

Audio signals

0.5V RMS, <1K output impedance, >10K input impedance.

Red, Green, Blue

0.7Vpp ±2dB, 75R input and output impedance. Note that the Red connection (pin 20) can alternatively carry the S-VHS Chrominance signal, which is 0.3V.

Composite Video / CSync

1Vpp including sync, ±2dB, 75R input and output impedance.Bandwidth = 25Hz to 4.8MHz for normal TV Video de-emphasis to CCIR 405.1 (625-line TV)

Fast Blanking

75R input and output impedance. This control voltage allows devices to over-ride the composite video input with RGB inputs, for example when inserting closed caption text. It is called fast because this can be done at the same speeds as other video signals, which is why it requires the same 75R impedances.

0 to 0.4 V: TV is driven by the composite video input signal (pin 19).Left unconnected, it is pulled to 0V by its 75R termination.

1V to 3 V: the TV is driven by the signals Red, Green, Blue and composite sync. The latter is sent to the TV on pin 19. This signal is useful when using a TV to display the RGB output of devices such as home computers with TV-compatible frame rates. Tying the signal to 5V via 100R forms a potential divider with the 75R termination, holding the signal at around 2V. Alternatively, if a TTL level (0 to 5V) negative sync pulse is available, this will be high during the display periods, so this can drive the blanking signal via a suitable resistor.

Control Voltage

0 to 2V = TV, Normal.

5 to 8V = TV wide screen

9.5 to 12V = AV mode

11. CIRCUIT DESCRIPTION

11.1 POWER SUPPLY:

· Socket PL800 is the 220VAC input.

· 3.5A fuse F800 is used to protect the device against short circuit and unexpected overloads.

· Line filter and capacitors L800, C801 and C803 are used to block the parasitic coming from the mains. They also prevent the noise, produced in the circuit, from being injected to the line.

· Voltage is rectified by using diodes D805 diode bridge. Using capacitor C815 (100uf) a DC voltage is produced. (310- 320VDC).

· The current in the primary side of the transformer TR800 comes to the SMPS IC (IC800 MC44608). The SMPS IC has a eight-pin DIP-8 package and an external MOSFET with a cooler is mounted on it. It has a built-in oscillator, overcurrent and overvoltage protection circuitry and runs at 100kHz. It starts with the current from the primary side of the transformer and follows the current from the feedback winding.

· Feedback current is deteceted by optocoupler IC803. Depending on the control current coming from the secondary side, SMPS IC keeps the output voltage constant by controlling the duty cycle of the ~30kHz signal (PWM) at the primary side of the transformer.

· Voltages on the secondary side are as follows: +30 Volts at D811, +8 Volts at D808, +15V at D810, -22 Volts at D812, +12Vst at Q804.

· Using the output of the D808, a photo diode inside of the IC803 generates feedback signal bu using optocoupler's photo transistor. This photo transistor adjusts the control voltage at the IC800 pin3. The voltage at this pin effects the pwm output frequency on the IC800 pin5. And finally output voltages reach their correct values by this way.

· Voltage regulator IC805 (LM7805) supplies +5 Volts, IC807 supplies +5V (off on standby mode), IC809 supplies +3.3V (by using output of the IC807, off on standby mode), Q804 supplies +12Vst, IC806 supplies +12V (off on standby mode), Q808 supplies -5V, D812 supplies -22V. Standby mode controlled by standby control transistors Q805, Q806, Q807.

· –22 Volts is used to feed the VFD (Vacuum Fluorescent Display) driver IC on the front panel. Using diode R844, –22V is decreased and connected to the filament winding to produce the DC offset for the filaments.

11.2 FRONT PANEL:

· All the functions on the front panel are controlled by IC300 (MT1379) on the mainboard

·IC300 sends the commands to IC101 uPD16311 via socket PL101 (pins 2,3 and 4).

· There are 16 keys scanning function, 2 LED outputs, 1 Stand-by output and VFD drivers on IC101.

· Pin 52 is the oscillator pin and is connected via R107 56K.

· LED D1 is blue in stand-by mode and off when the device is on.

· Vacuum fluorescent display MD1 is specially designed for AV2300.

· The scanned keys are transmitted via IC101 to IC300 on the mainboard.

· IR remote control receiver module IC102 (TSOP1836) sends the commands from the remote control directly to IC300.

· Socket PL102 carries the VFD filament voltage and –22 Volts.

11.3 I/Os and Back Panel:

- There are 2 SCART connector , 6 pieces RCA jacks, for audio output, 1 optical digital audio ,1 s-video output on the back panel.

- TOTX178 is used for laser output.

- For optical audio output S/PDIF is used.

- Q620, Q621 transistors are to mute the audio outputs while switching the state of the unit (power on/of)

- SCART pin 8 controls 16:9 and 4:3 mode .

- When the pin 8 output of the scart becomes 5 volts, 4:3 mode is selected and 16:9 mode is selected when this is turned off.

- There are antenna inputs for AM/FM tuner.

11.4 DDX Board (Class-D Amplifier):

· Chipset : 1xDDX-8228 + 2x DDX-2050

· Architecture : 1xFull-Bridge + 5xHalf -Bridge

· Power Supply : + 30V unipolar supply @ 6A max., + 3.3V @ 0.1A typ.

· Audio Input Interface: Serial I2S

· Control Interface: I2C

· Power Interface: + 30V @ 6A Max., + 3.3V@ 0.1A Typ

· Output Interface: Speaker Level

· Speakers: 4 OhmSatellites + 8 Ohm Subwoofer

· Output Power: 5x15 Wrms + 1x25 Wrms

· DDX Audio proccess IC is DDX-8228.

· DDX board have digital audio input with I 2 S bus.

· For mute function, EAPD (pin51, External Amplifier Powerdown) signalis used. This signal comes to the power output ICs U3 and U4 (DDX-2050 ICs Pin25) as power down signal.

12. SOFTWARE

12.1 UNIVERSAL SERVICE PASSWORD

- Universal Password for Parental level is **1369**

12.2 VERSION PAGE (Hidden Menu)

To see Version Page:

- Press DISPLAY button from remote for Setup Menu

- Press "1"-"3"-"5"-"7" at Setup Menu

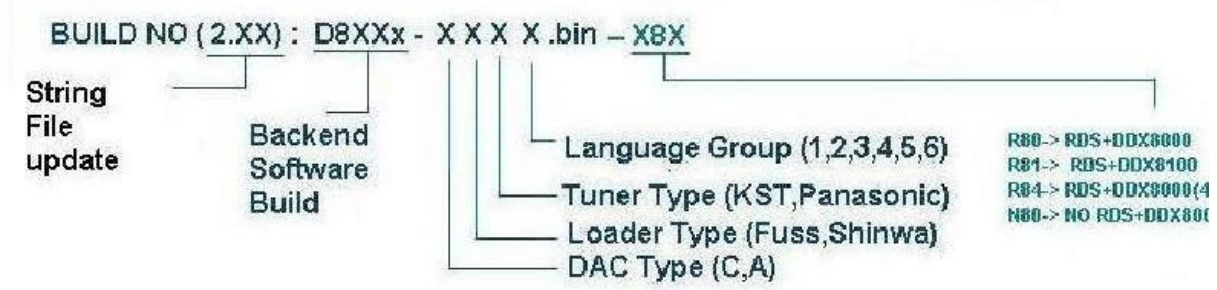
- Setup Menu screen refresh and "Version" selection can be seen under "Preferences Setup"

- Select "Version" for version page

-BUILD NO contains version and Hardware option other information for development only.

- Details of Build No as follows:

Tracking Build number and Hardware options from Version Page:



Language Groups for AV13XX Receivers:

	Group 1	Group 2	Group 3	Group 4	Group 5	Group 6
1	English	English	English	English	English	English
2	French	Italian	Danish	Czech	Slovenian	German
3	German	Portugues	Swedish	Polish	Romanian	Dutch
4	Dutch	Spanish	Finnish	Hungarian	Crotarian	Turkish

- Press "DISPLAY" button on remote control to exit menu.

12.3 VFD FULL SEGMENT TEST MODE

During Pressing “STOP” button on Front Pannel if you press Standby button all segments of VFD are higligted.

12.4 REGION MANAGEMENT

At Version page by using arrow keys Region can be changed.

12.5 UPDATE FILE NAME

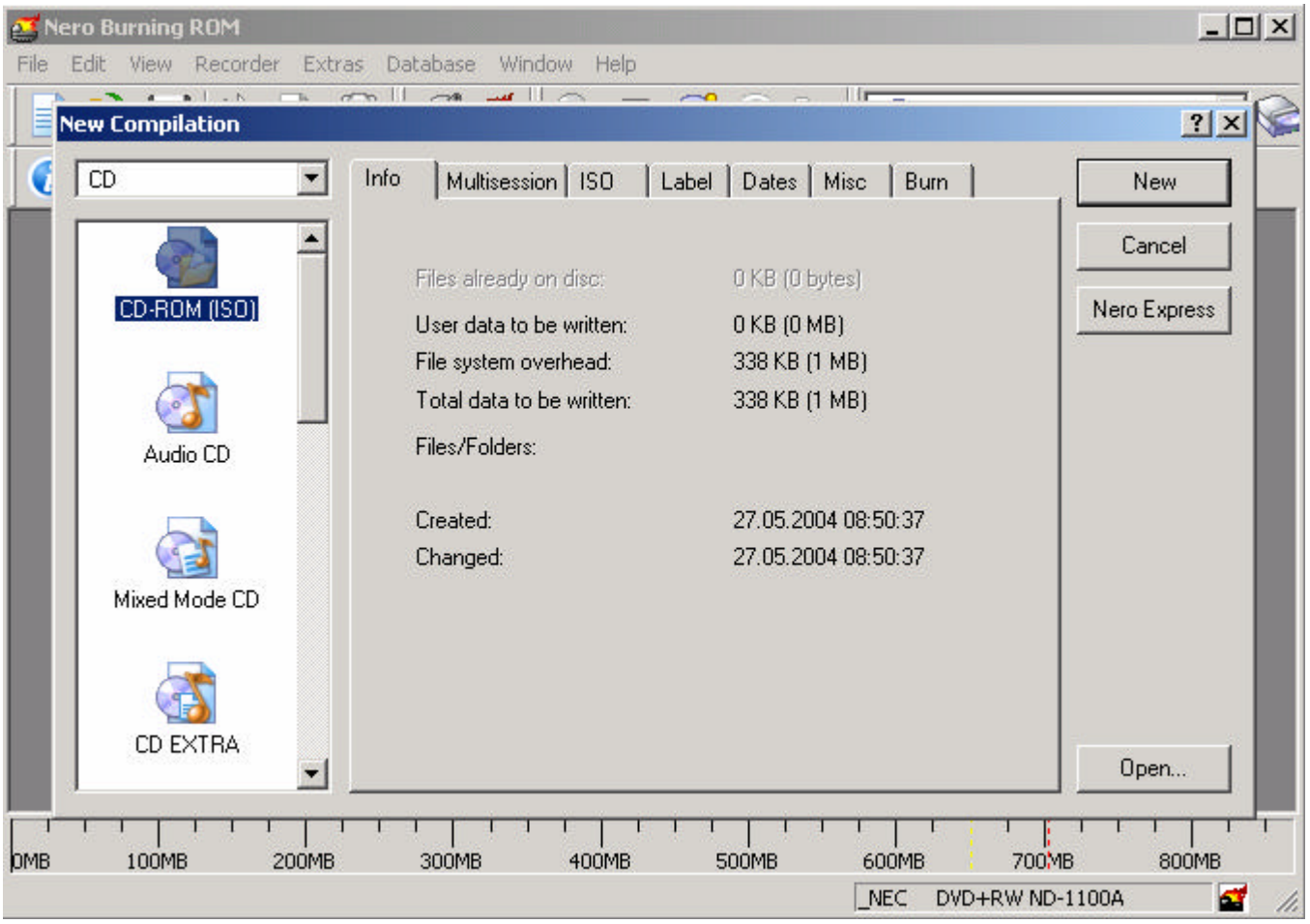
Proper Update file name can be learned from Version Page as follows:
First Characters of DAC, LOADER, TUNER and LANGUAGE group gives proper update file name.
Example: CFK.bin

12.5 CD UPDATE PROCEDURE

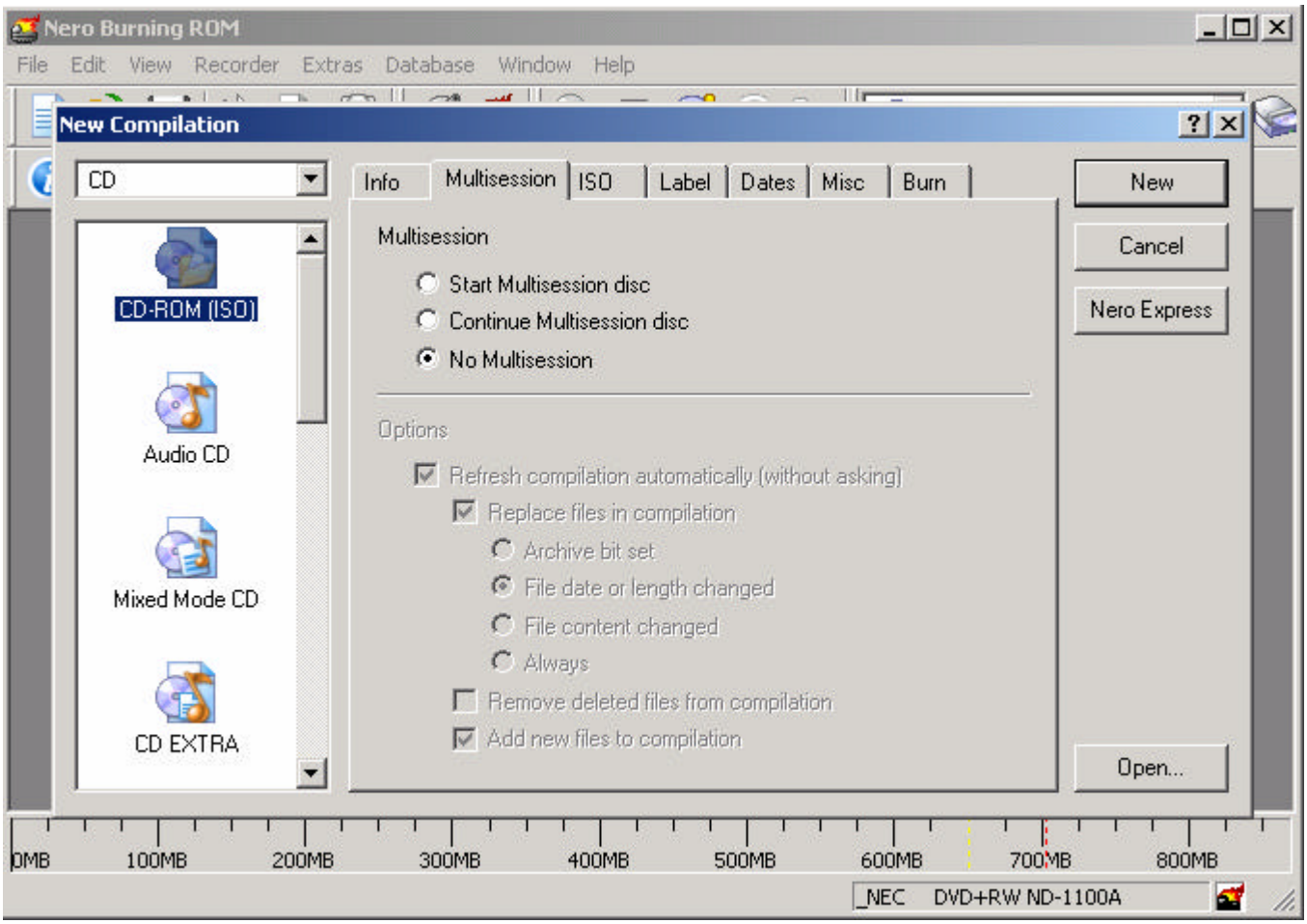
1) Player can be updated automatically with Update CD which contains proper file.
Check hidden menu for update file name.
2) Burn CD* within proper update file
3) There should be no Volume Name for CD
Open Tray and place update CD
4) You can see
5) Press Play button to start upgrade
6) You can see “File copying” OSD message for a few second
7) Tray is open automatically
8) No need for CD in tray; Take it from away
9) During upgrade procedure “CD upgrade start, Please wait..” indicator at OSD, and “UPG” indicator at VFD
10) Upgrade procedure takes about a few minutes, please wait if tray is open
11) When CD update is finished tray is closed, screen is refreshed, update is finished

NOTE: * For “NERO Burning Rom” program

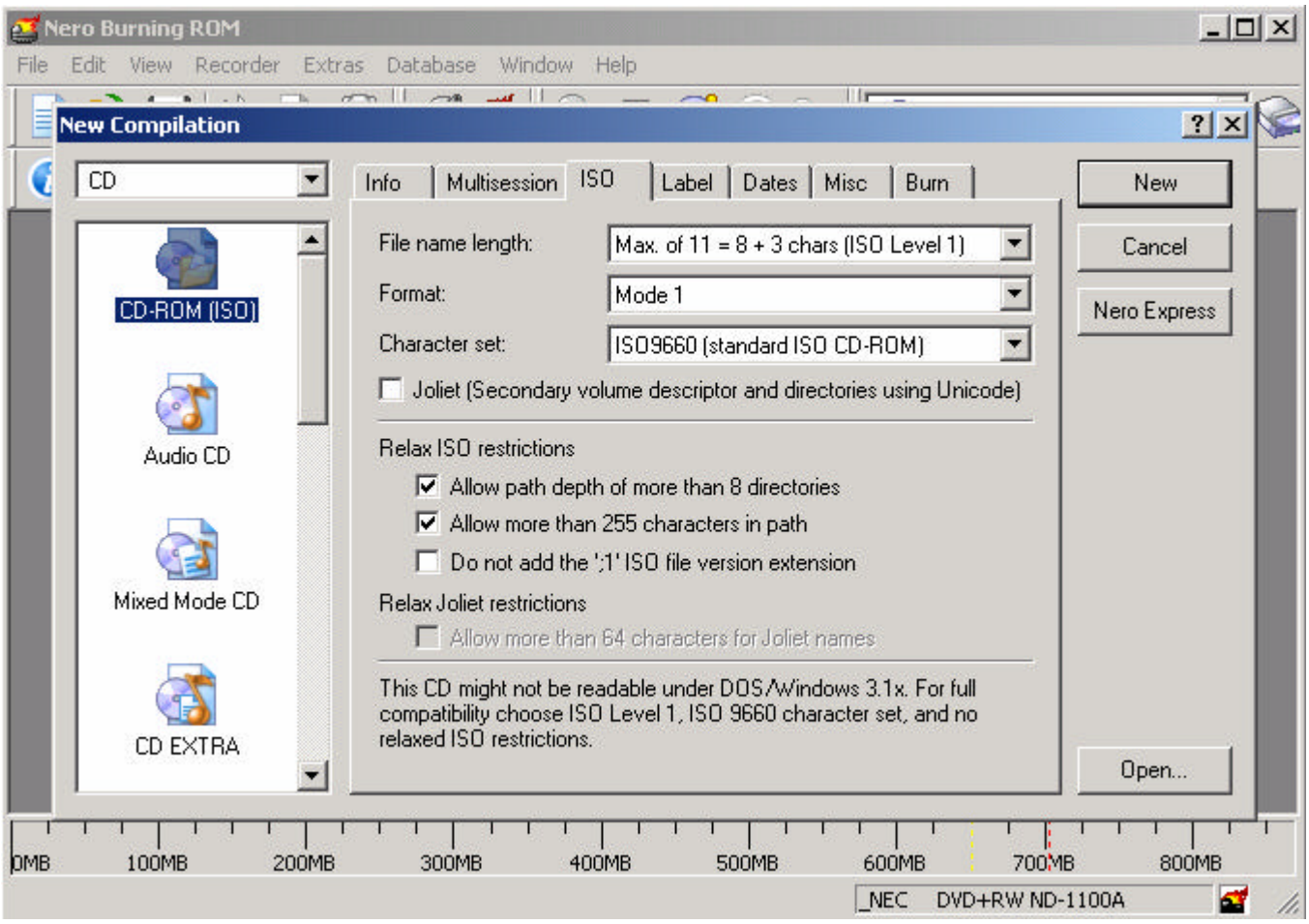
Ideal configuration;
Multisession selection should be “No Multisession”
File format should be “ ISO9660”. Do not use “Joliet”
It is better to erase with “Quick Erase” if you use CD-RW before burning
There should be no Volume lable
It may be better to put some dummy files sn CD update file



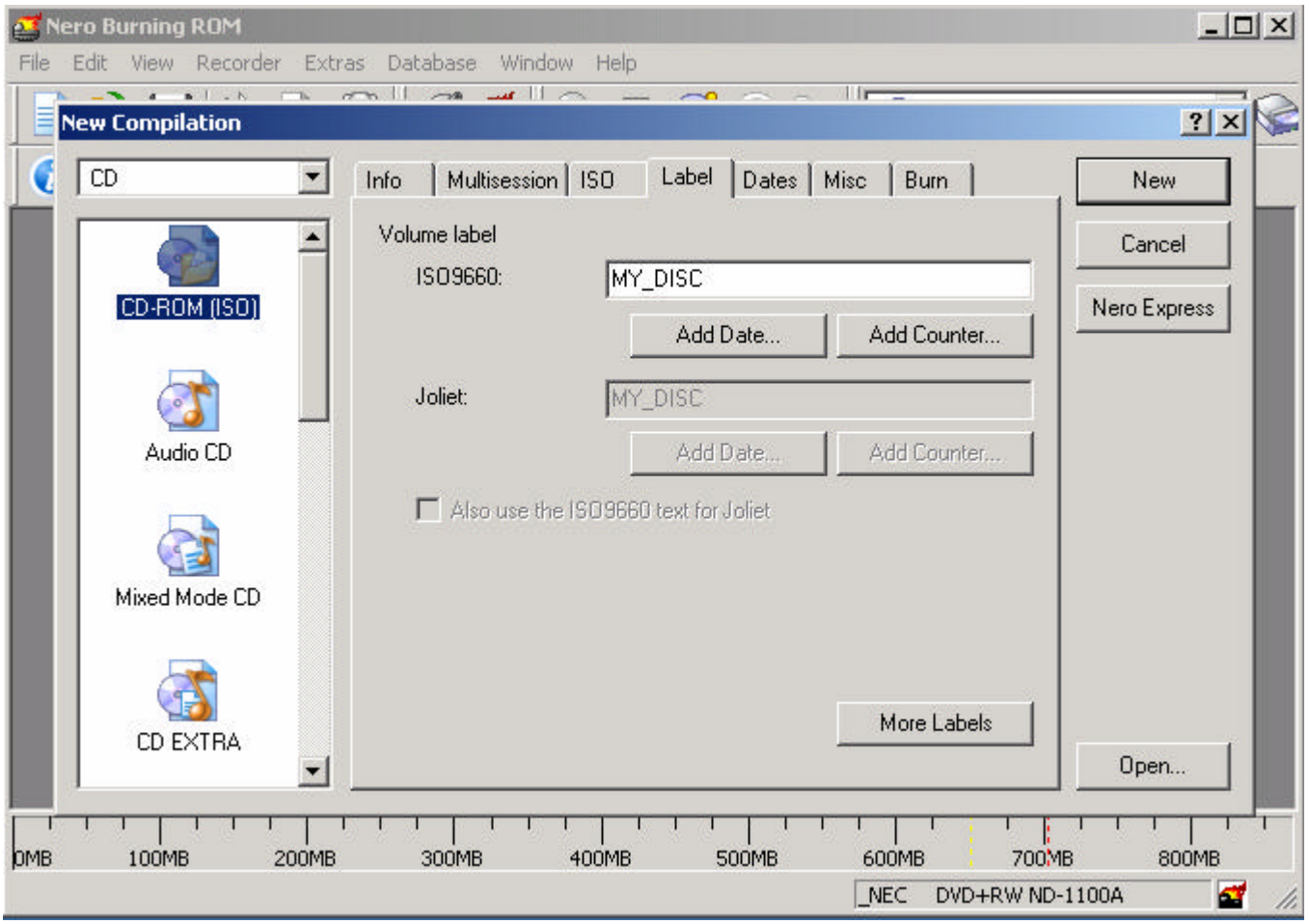
Pay attention the left side. Select **CD and CD_ROM (ISO)** on the upper left side of screen

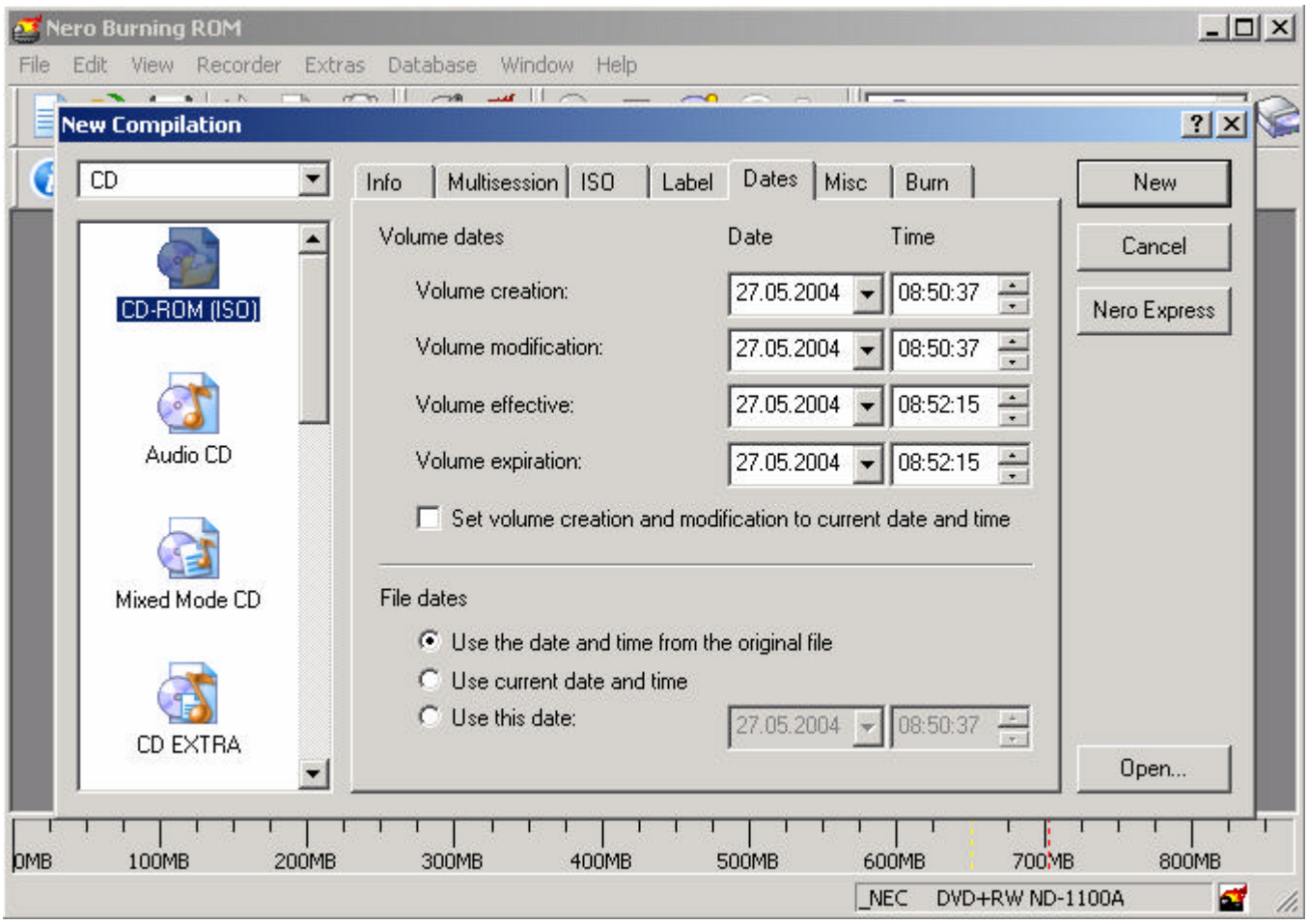


Select **No Multisession**

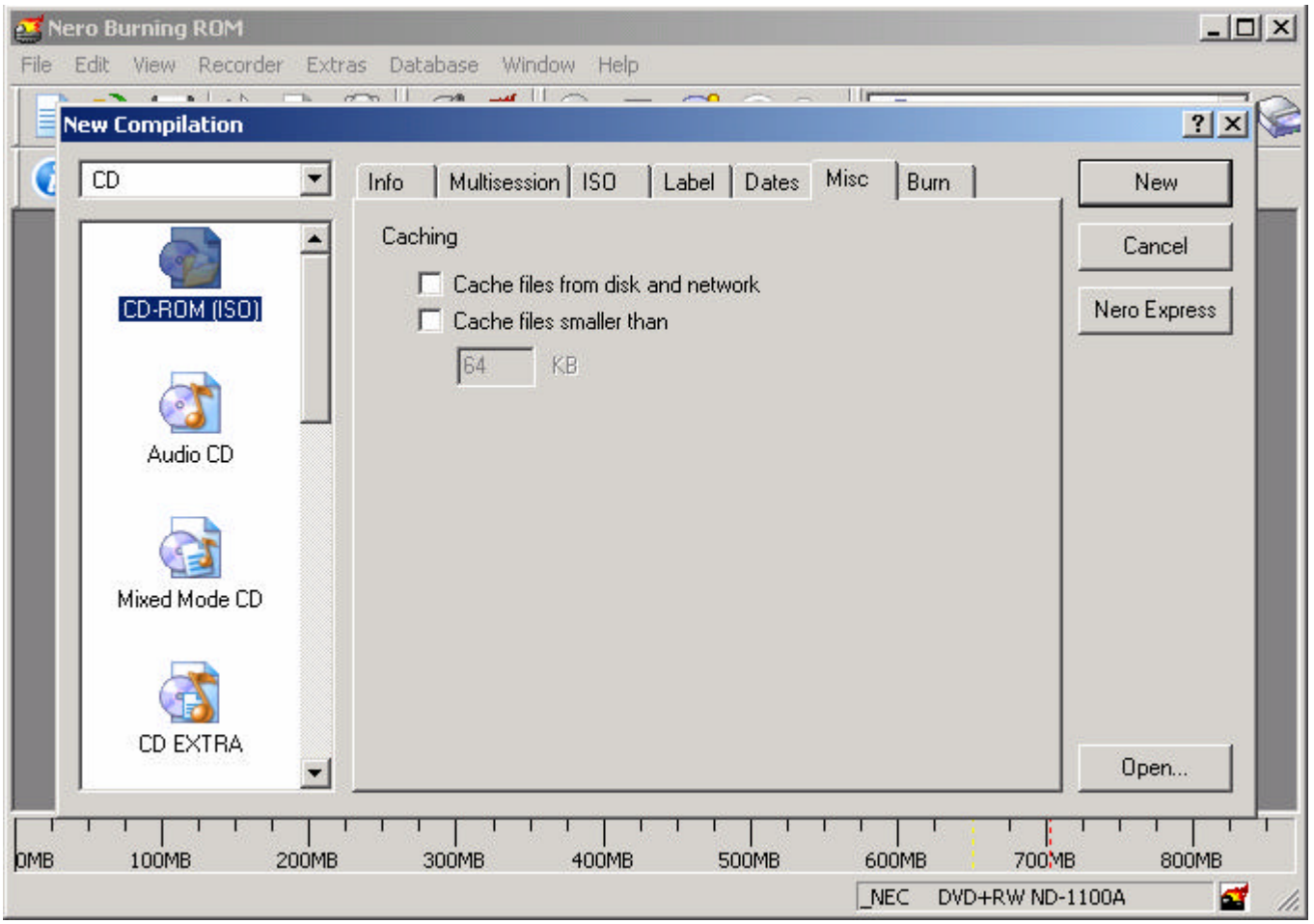


Format is **Mode 1**

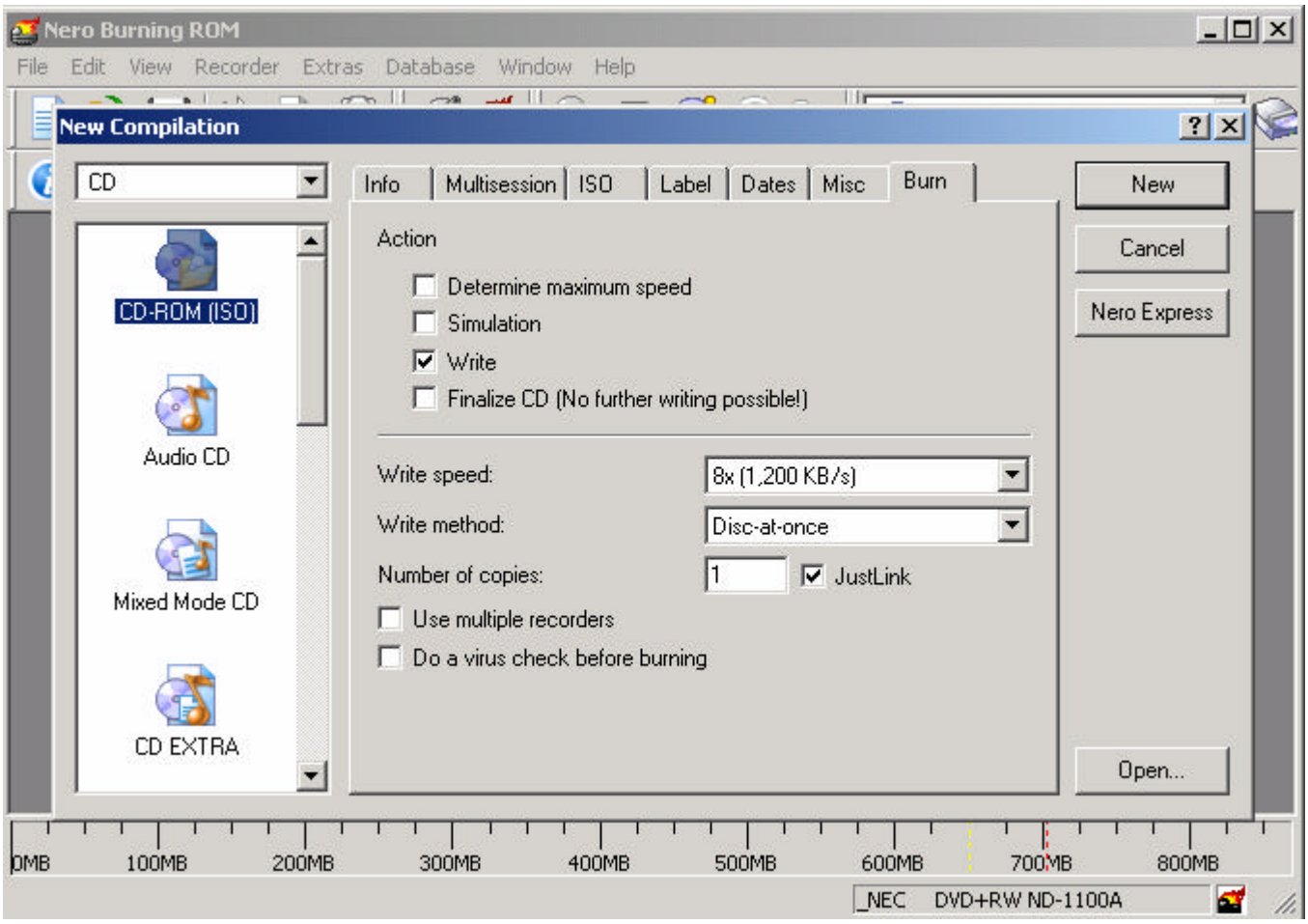

Nero Burning ROM
File Edit View Recorder Extras Database Window Help
New Compilation
CD
CD-ROM (ISO)
Audio CD
Mixed Mode CD
CD EXTRA
Info Multisession ISO Label Dates Misc Burn
Volume label
ISO9660: MY_DISC
Add Date... Add Counter...
Joliet: MY_DISC
Add Date... Add Counter...
Also use the ISO9660 text for Joliet
More Labels
New
Cancel
Nero Express
Open...
0MB 100MB 200MB 300MB 400MB 500MB 600MB 700MB 800MB
_NEC DVD+RW ND-1100A



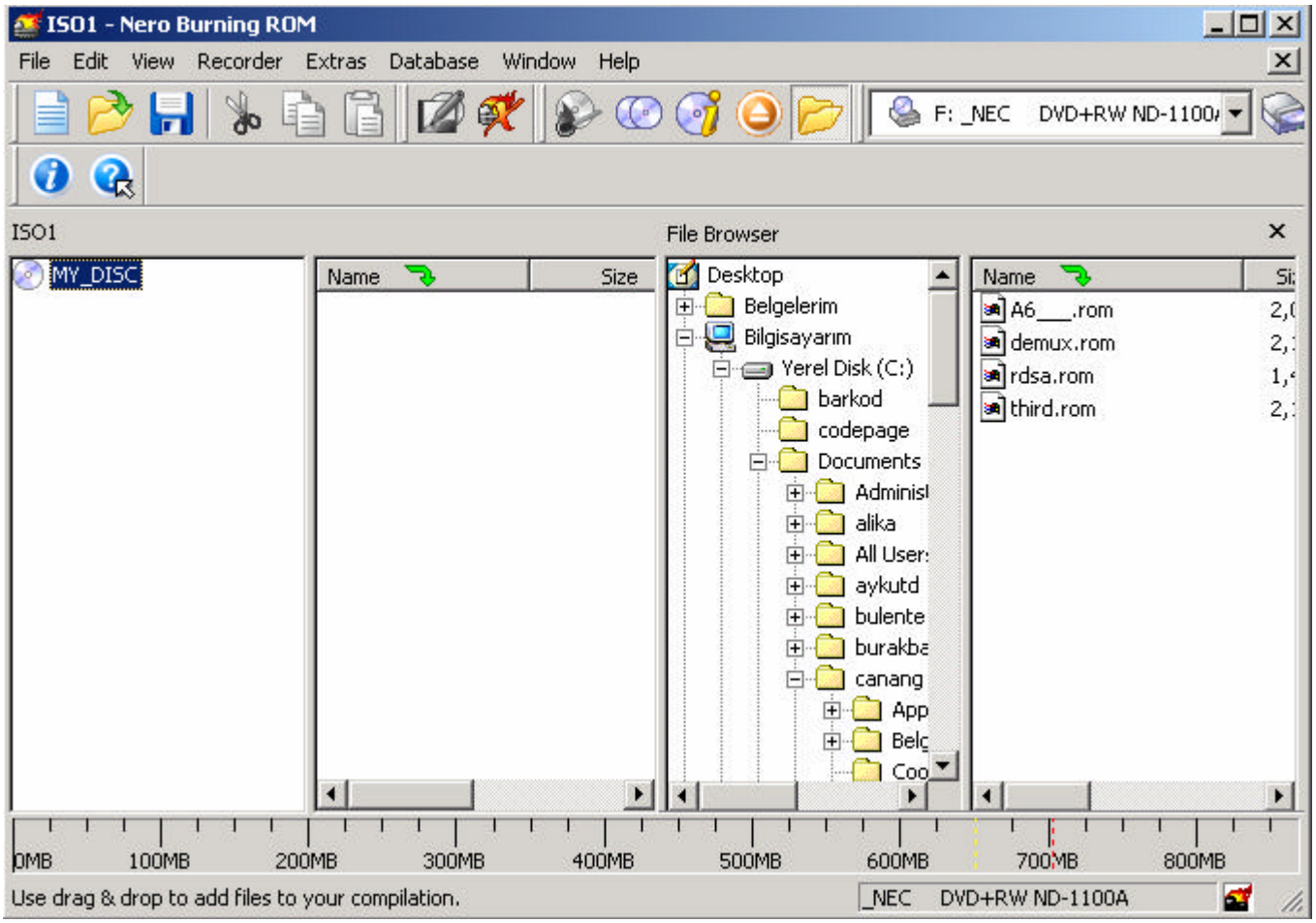
Leave the dates as it is



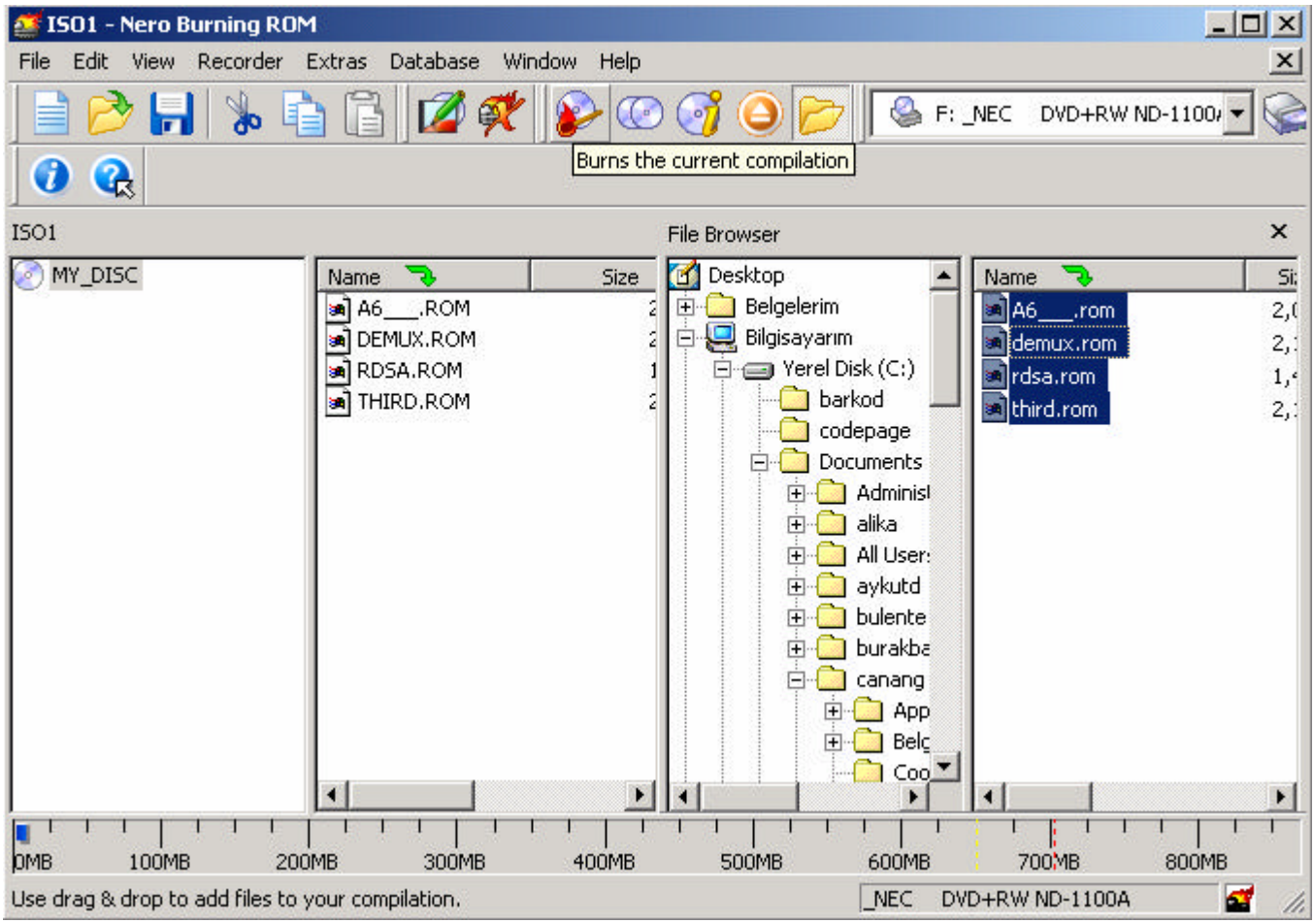
Leave it as it is



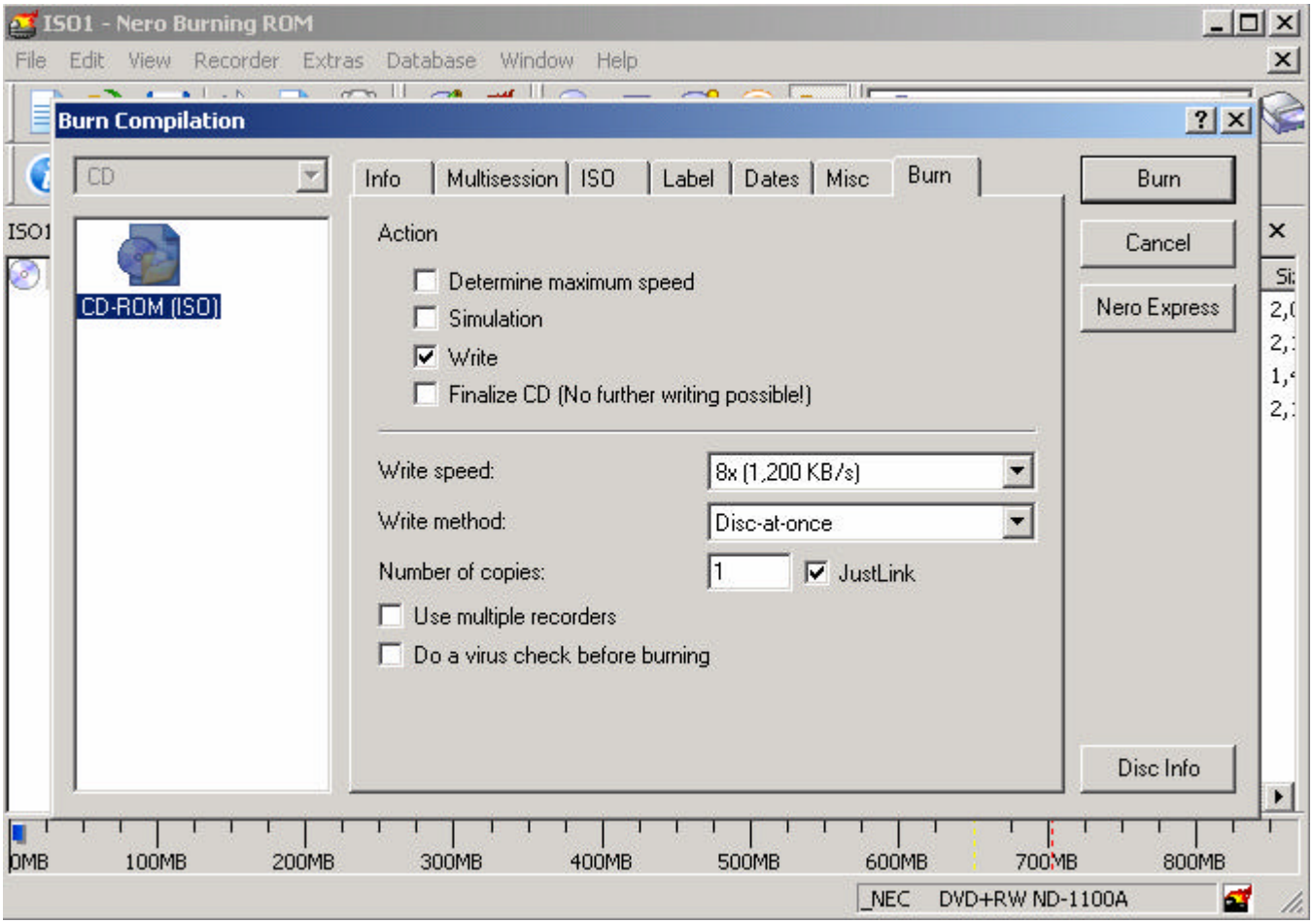
Click the “New” on the upper right corner of the screen



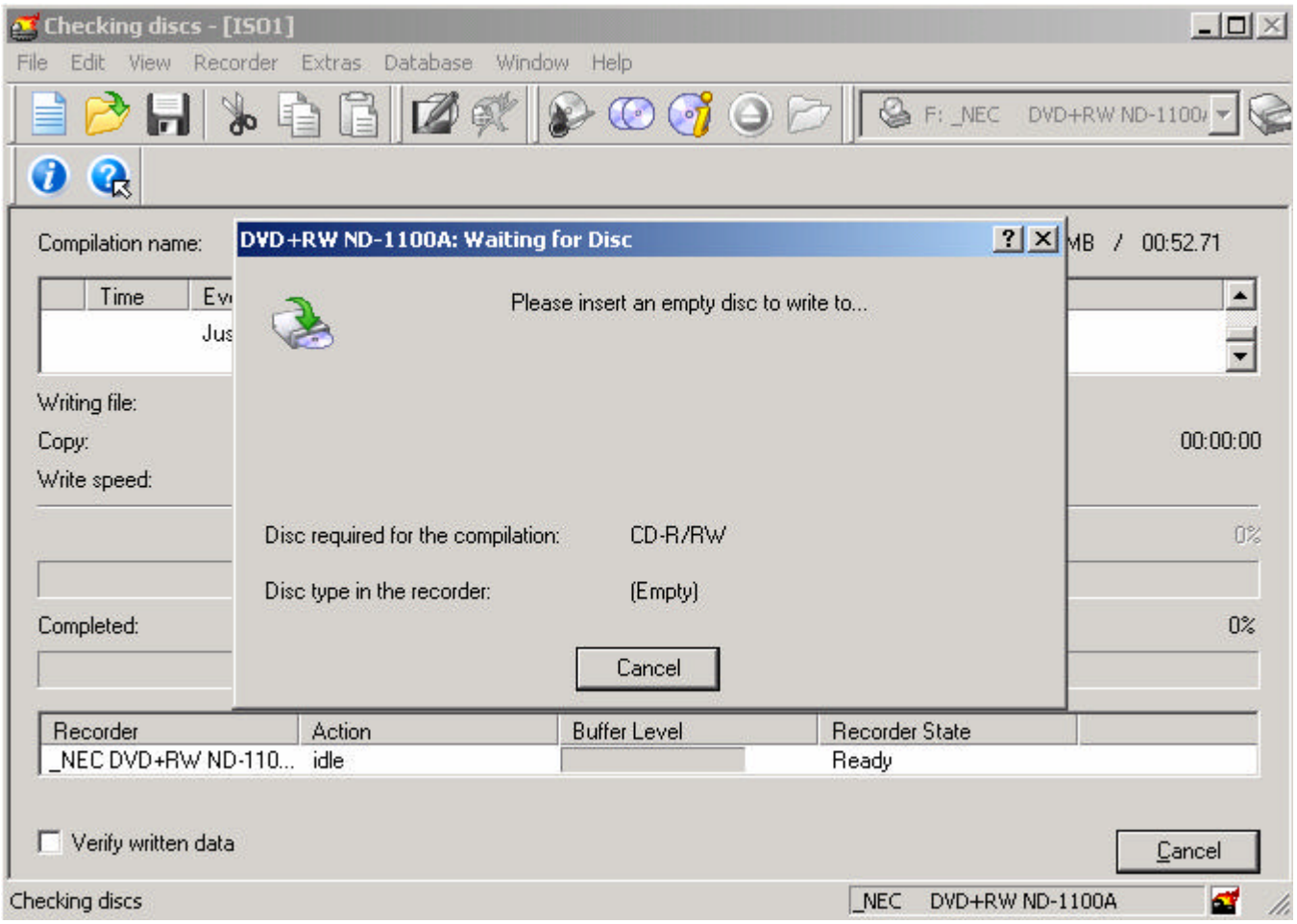
Select your file from file browser then you will see your file in the “Name” section on the right side and then copy the files to under “Name” section on the left side.(this is just an example you will see your file name when you are doing this process)



Click the “Burns the current compilation”

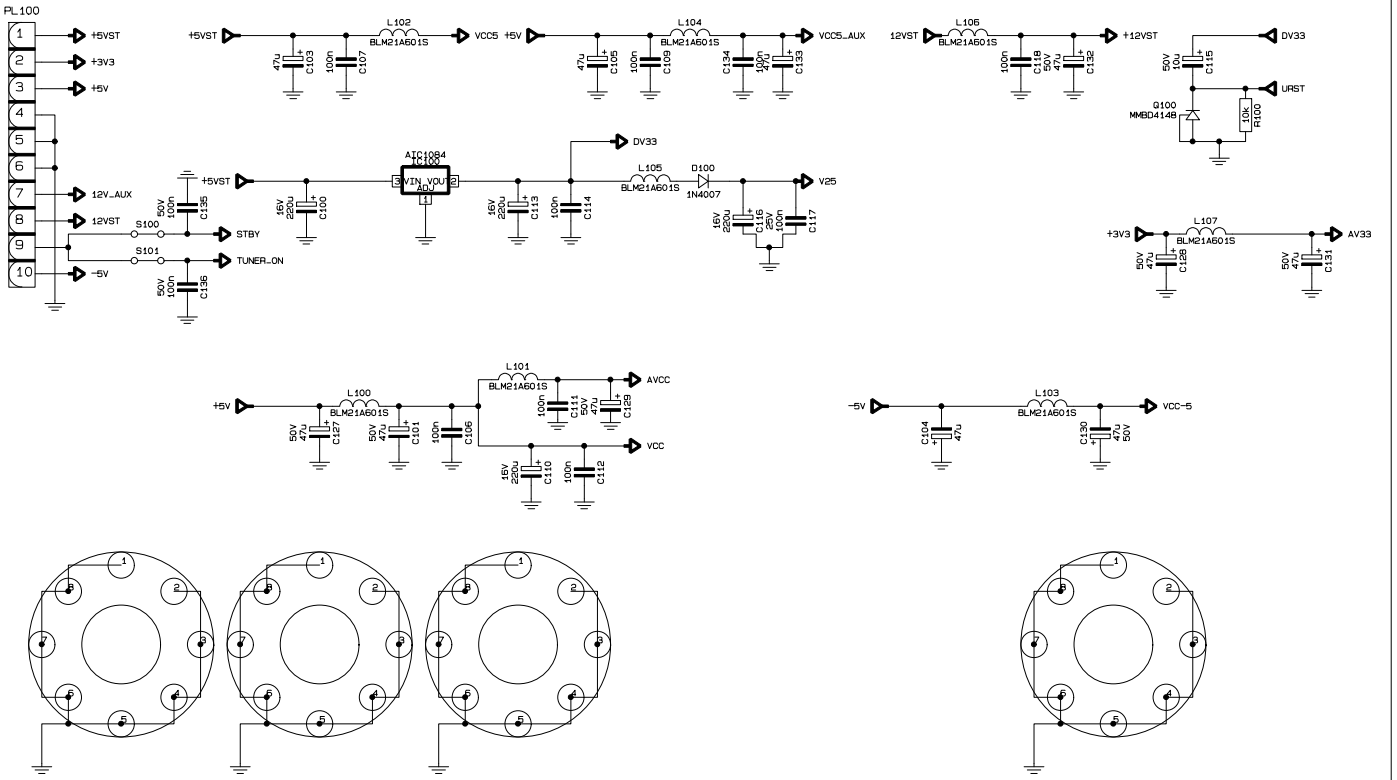


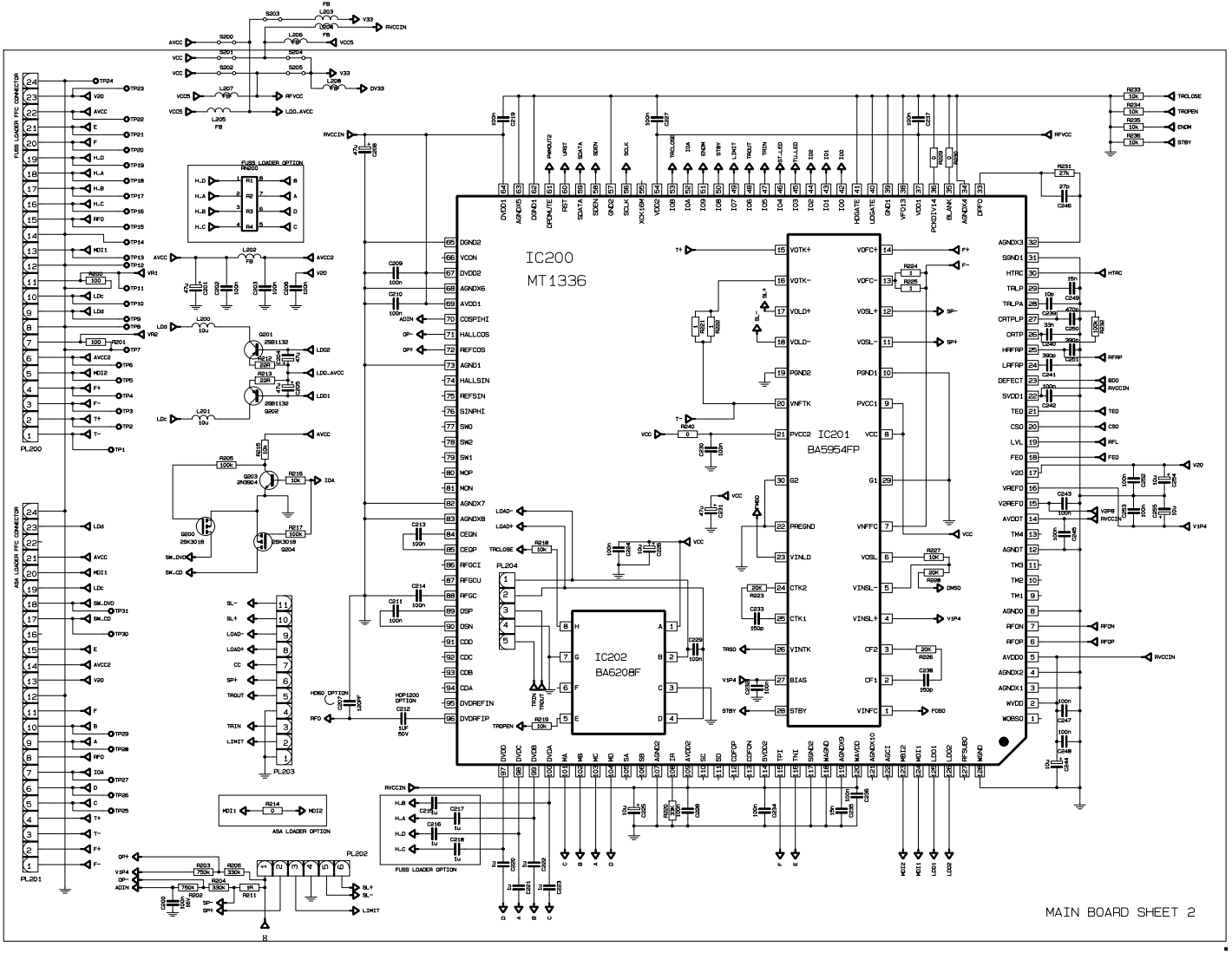
Then you will see this screen and click the “Burn” on the right upper side of screen

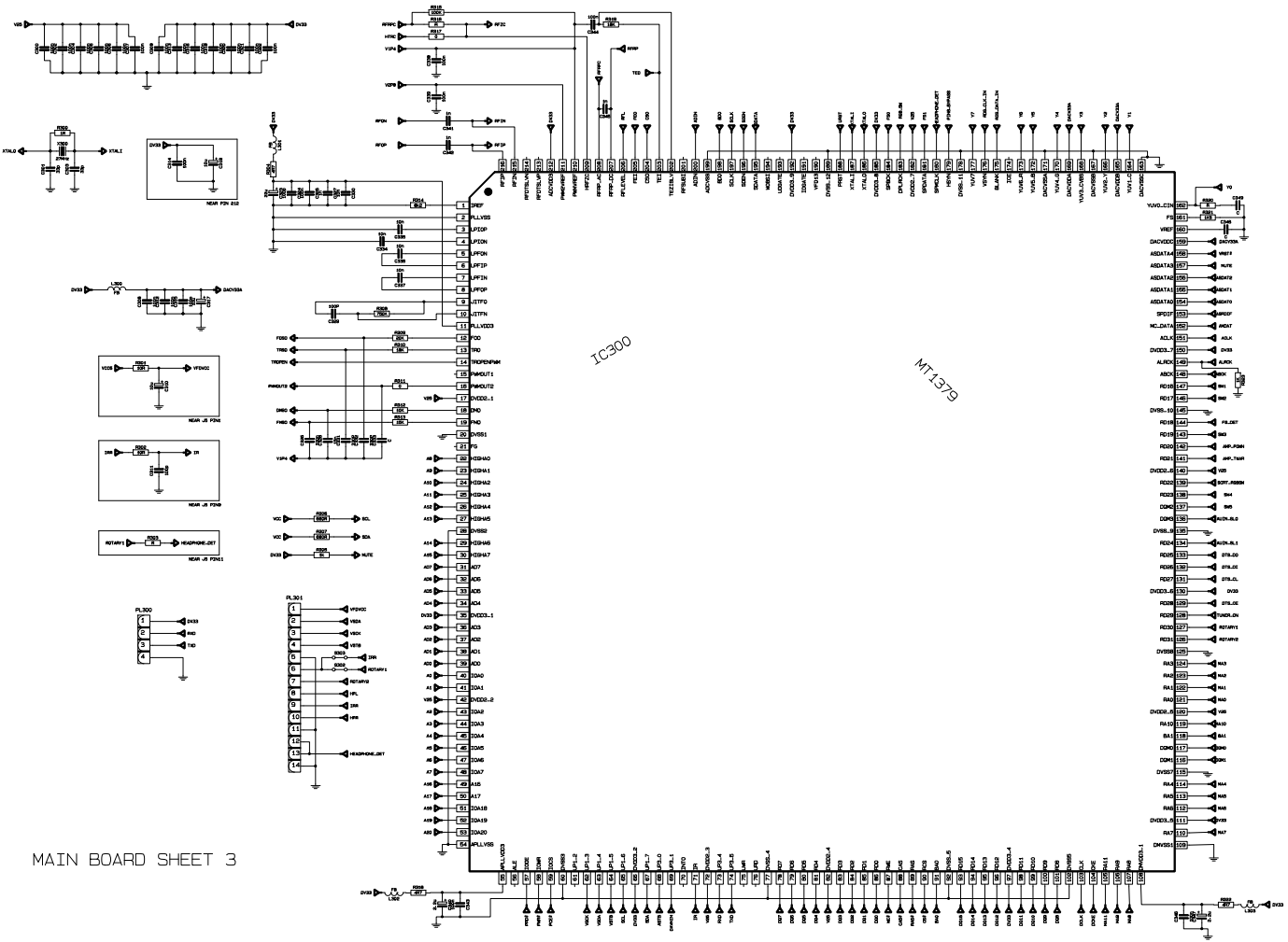


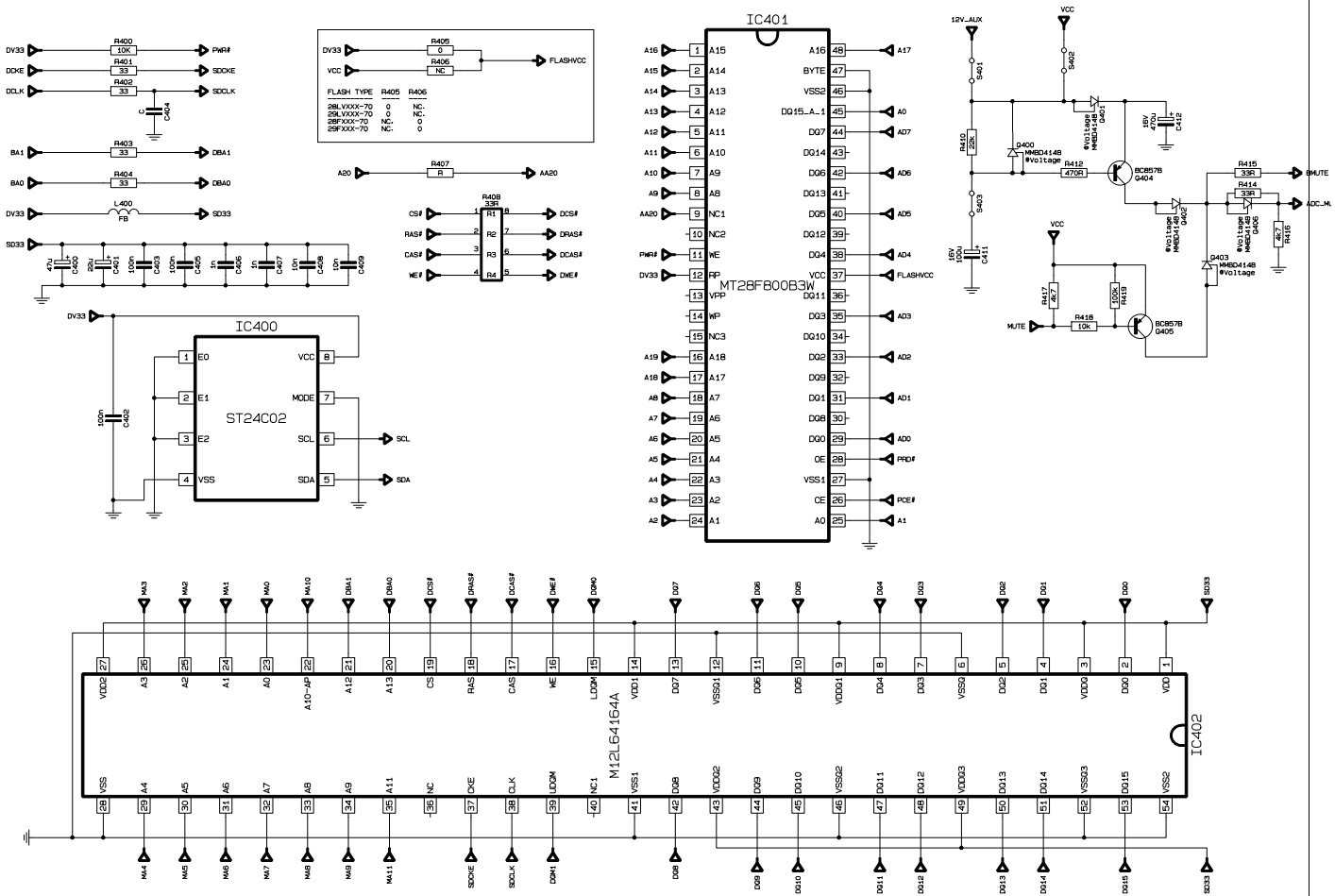
You will see this screen and tray will open itself on computer ,then place the CD in CD-ROM And it will start writing. At the end you will see “burn complited”

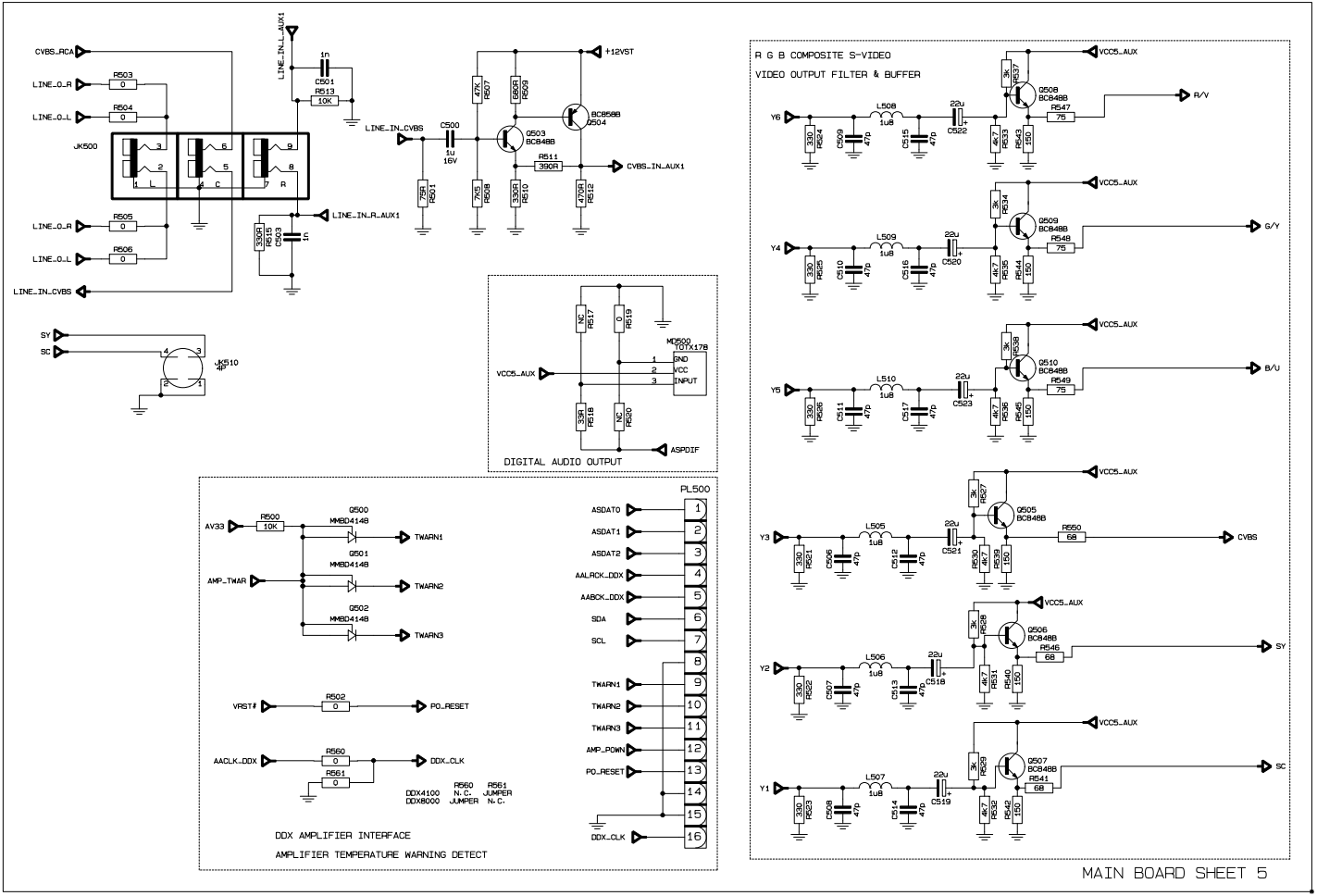
MAIN BOARD

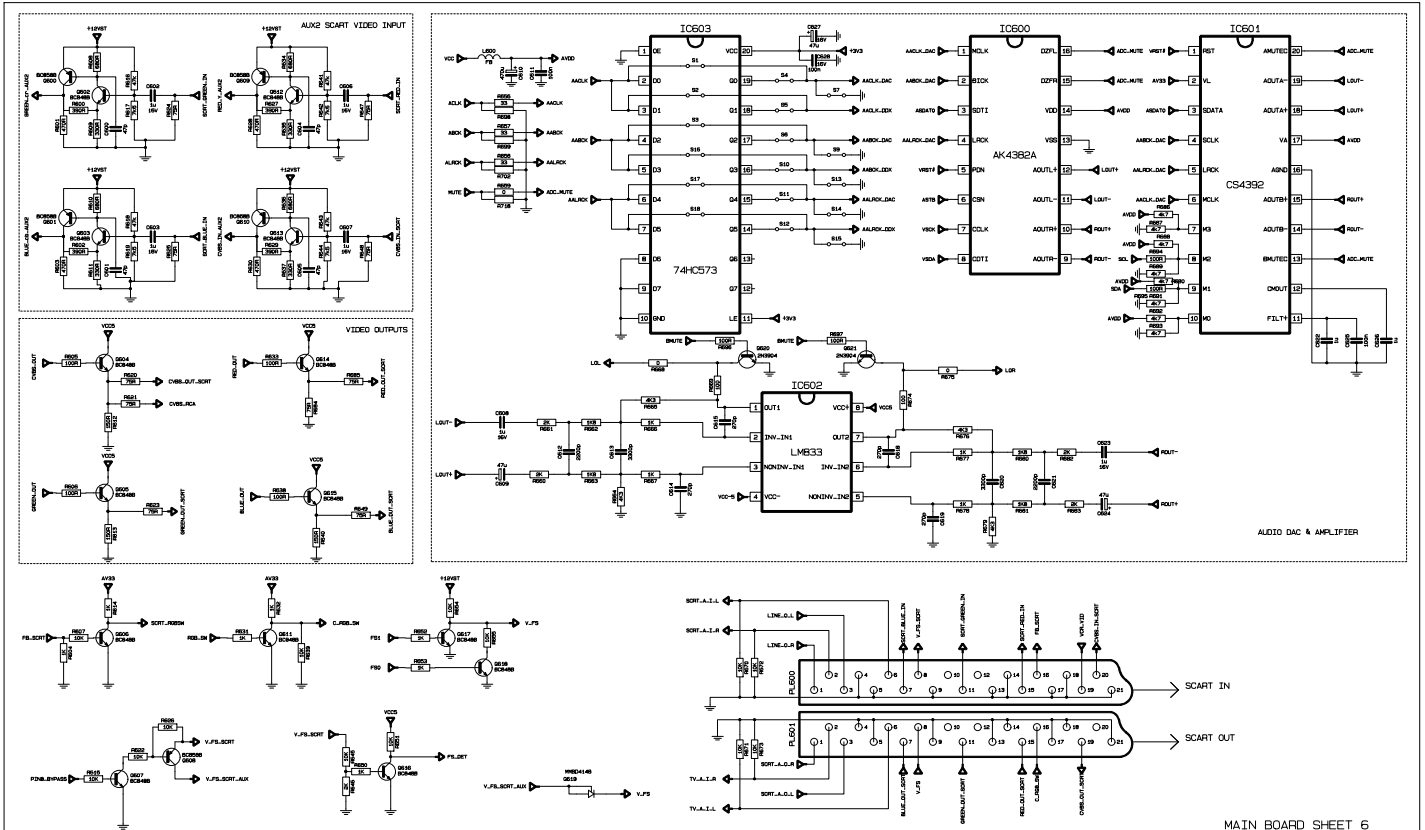

PL100
+5VST
+3V3
+5V
12V_AUX
12VST
S100
STBY
S101
TUNER_ON
-5V
L102
BLM21A601S
VCC5
L104
VCC5_AUX
L106
+12VST
DV33
URST
Q100
MMBD414B
R100
10K
AIC1084
IC100
VIN
VOU
ADJ
L105
D100
1N4007
V25
L107
+3V3
AV33
L101
AVCC
VCC
L100
L103
-5V
VCC-5
MAIN BOARD SHEET 1

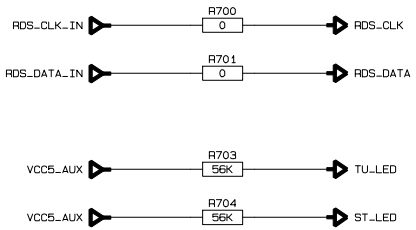

IC200
MT1336
IC201
BA5954FP
IC202
BA6208F
PL200
PL201
PL202
PL203
PL204
MAIN BOARD SHEET 2

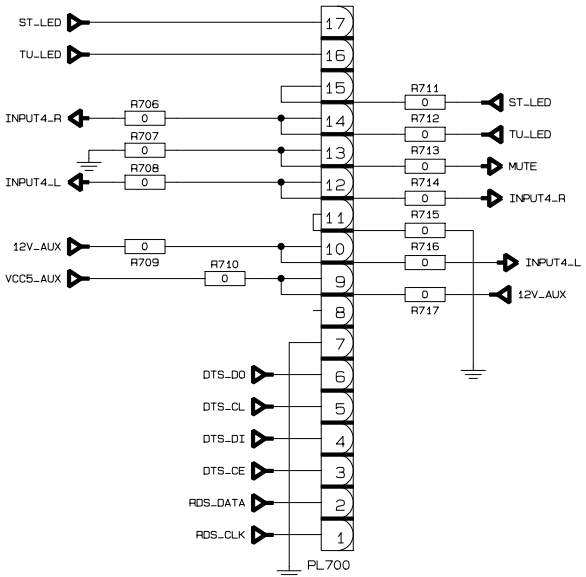

IC300
MT1379
MAIN BOARD SHEET 3


IC401
MT28F800B3W
IC400
ST24C02
IC402
M12L64164A
FLASH TYPE R405 R406
28LVXXX-70 0 NC.
29LVXXX-70 0 NC.
28FXXX-70 NC. 0
29FXXX-70 NC. 0
12V_AUX
VCC
MUTE
ADC_MUTE
MAIN BOARD SHEET 4

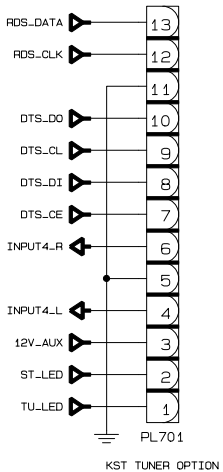

CVBS_RCA
LINE_O_R
LINE_O_L
JK500
LINE_O_R
LINE_O_L
LINE_IN_CVBS
LINE_IN_L_AUX1
LINE_IN_CVBS
LINE_IN_R_AUX1
+12VST
CVBS_IN_AUX1
SY
SC
JK510
4P
DIGITAL AUDIO OUTPUT
MD500
TOTX178
GND
VCC
INPUT
ASPDIF
VCC5_AUX
PL500
ASDAT0
ASDAT1
ASDAT2
AALRCK_DDX
AABCK_DDX
SDA
SCL
TWARN1
TWARN2
TWARN3
AMP_POWN
PO_RESET
DDX_CLK
AV33
AMP_TWAR
VRST#
AACLK_DDX
TWARN1
TWARN2
TWARN3
PO_RESET
DDX_CLK
DDX AMPLIFIER INTERFACE
AMPLIFIER TEMPERATURE WARNING DETECT
R G B COMPOSITE S-VIDEO
VIDEO OUTPUT FILTER & BUFFER
R/V
G/Y
B/U
CVBS
SY
SC
MAIN BOARD SHEET 5


AUX2 SCART VIDEO INPUT
VIDEO OUTPUTS
IC603
74HC573
IC600
AK4382A
IC601
CS4392
IC602
LM833
AUDIO DAC & AMPLIFIER
SCART IN
SCART OUT
MAIN BOARD SHEET 6





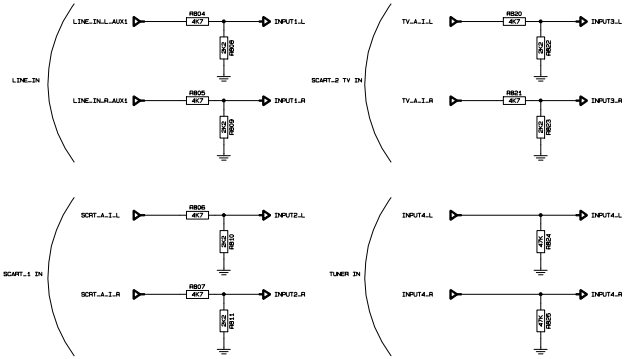
TBHK / PANASONIC TUNER OPTION

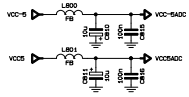


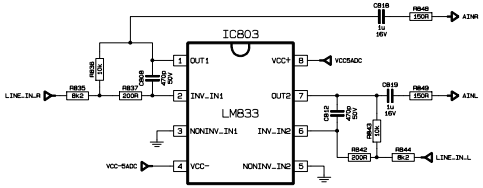
KST TUNER OPTION

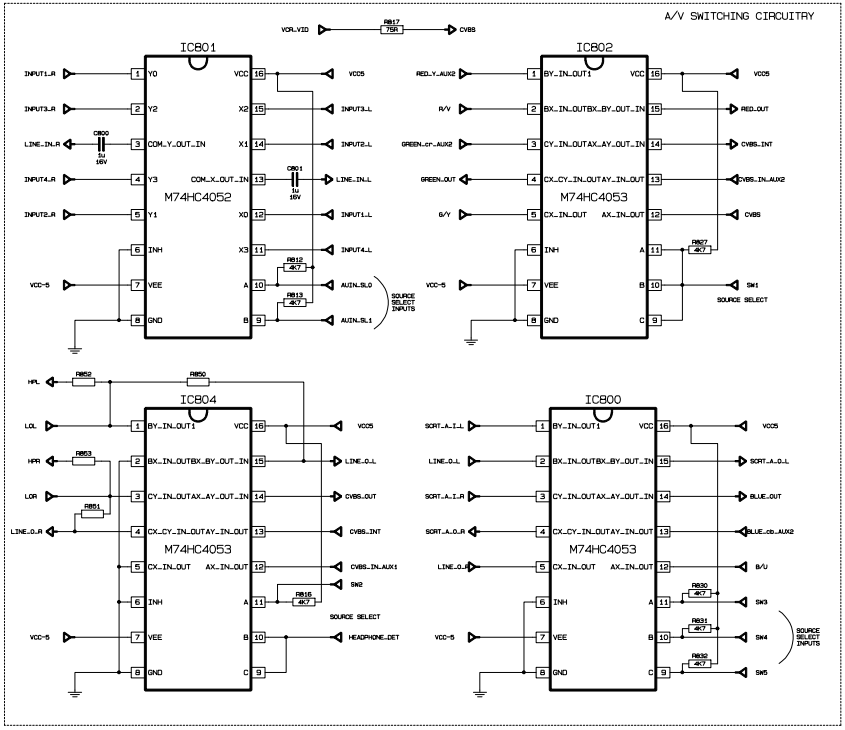
RESISTOR	PANASONIC	TBHK
R706	N.C.	JUMPER
R707	N.C.	JUMPER
R708	N.C.	JUMPER
R709	N.C.	JUMPER
R710	N.C.	JUMPER
R711	JUMPER	N.C.
R712	JUMPER	N.C.
R713	JUMPER	N.C.
R714	JUMPER	N.C.
R715	JUMPER	N.C.
R716	JUMPER	N.C.
R717	JUMPER	N.C.

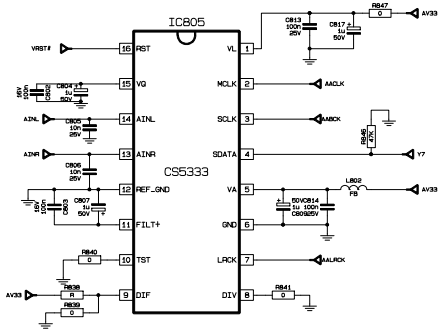
MAIN BOARD SHEET 7





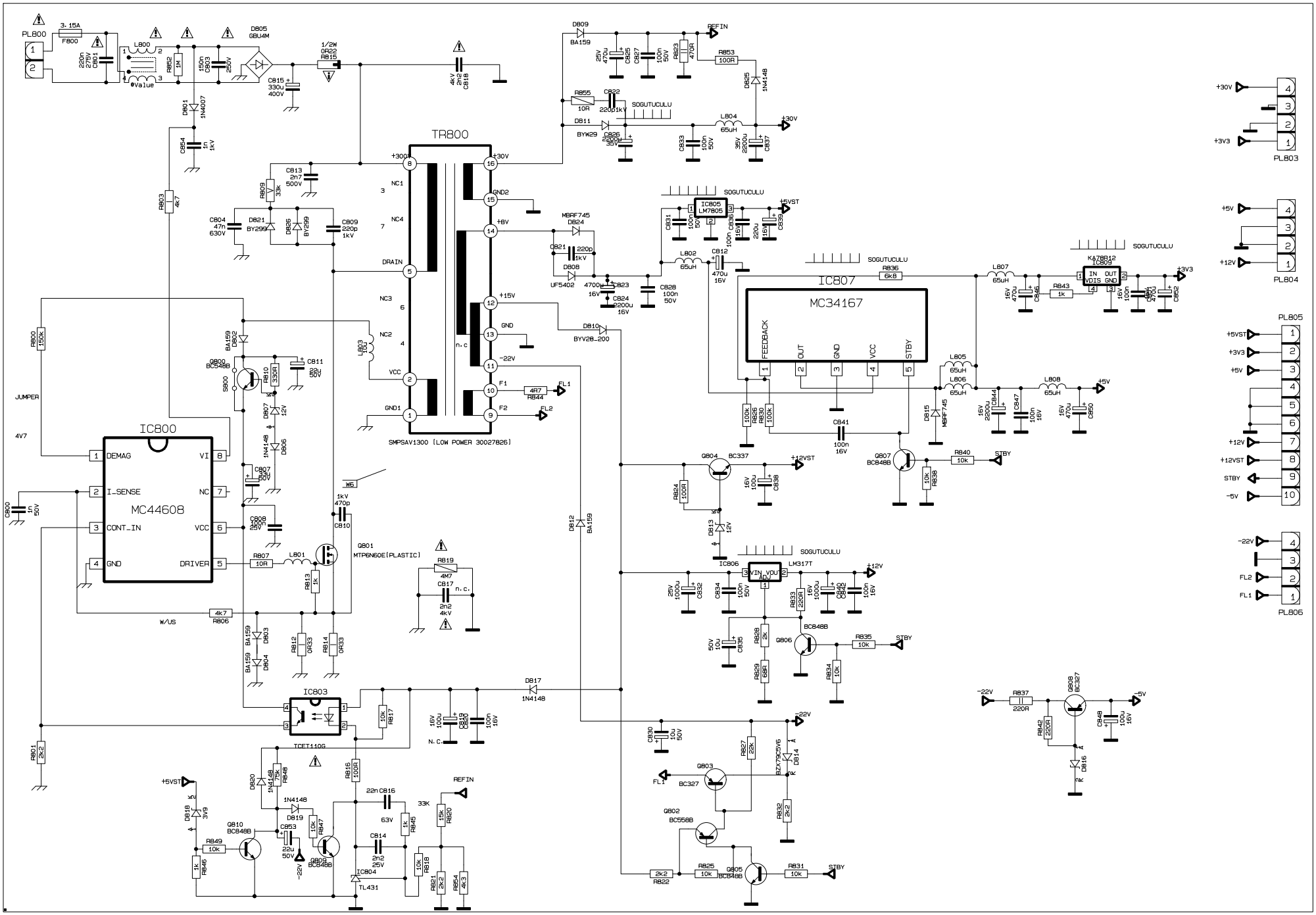




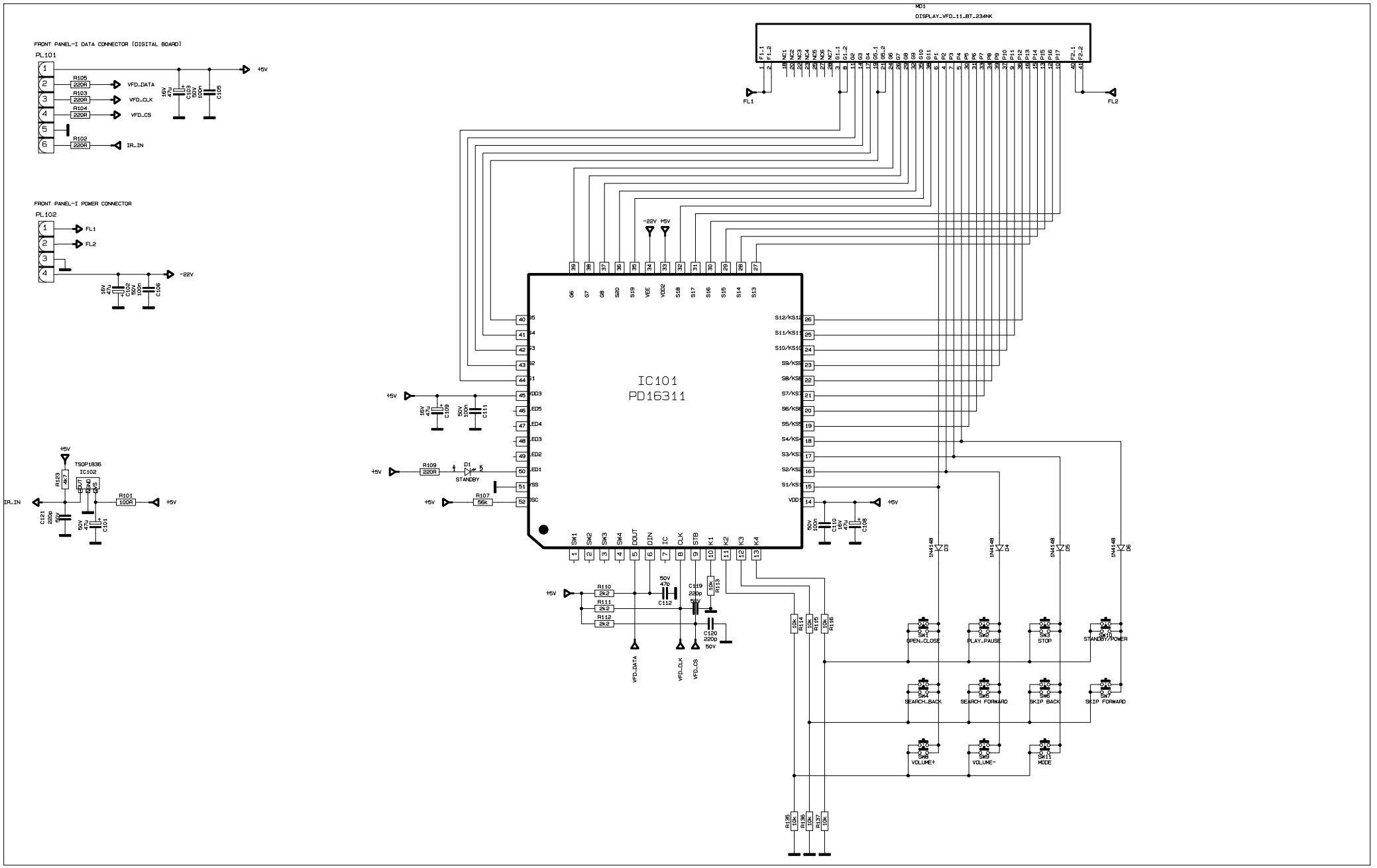


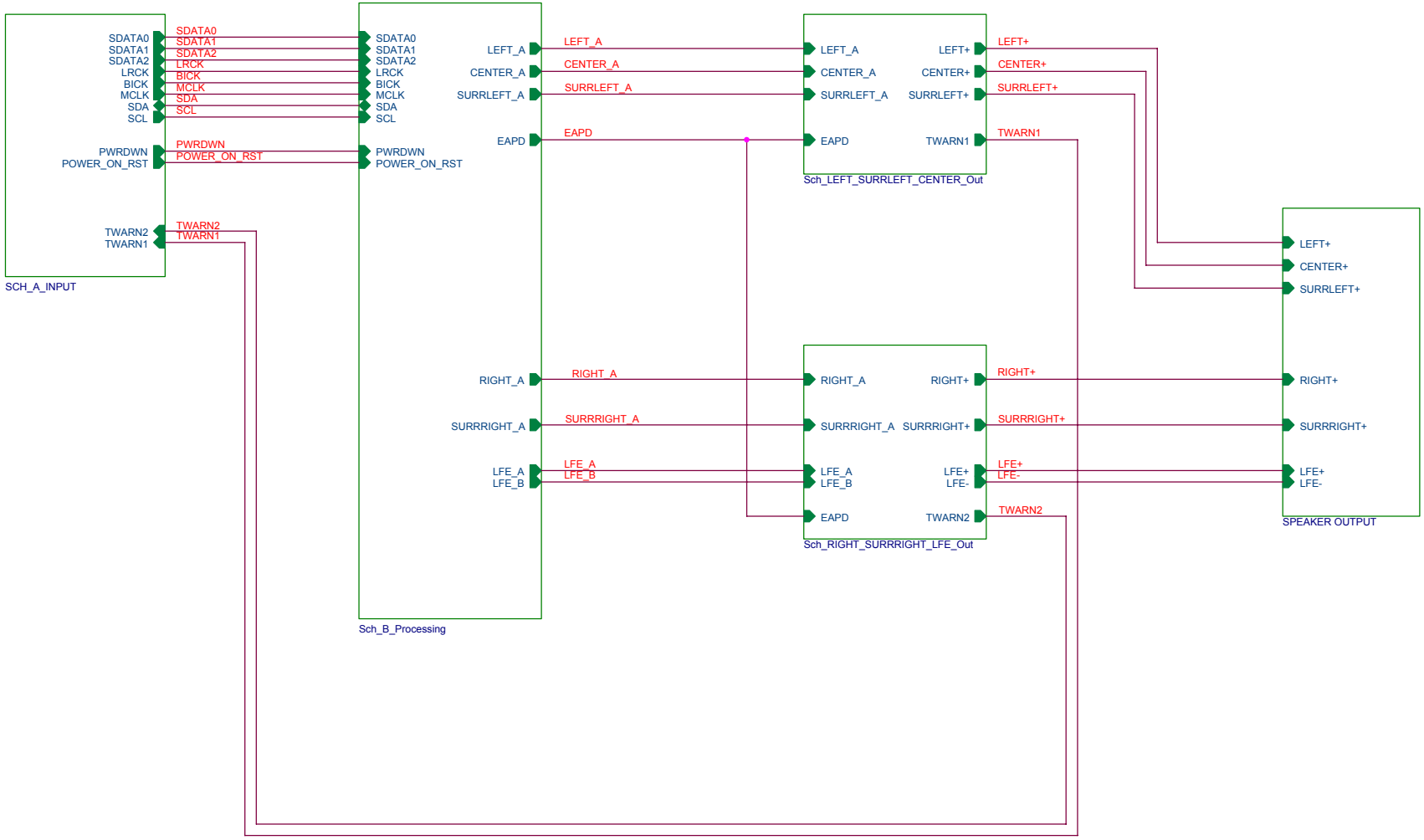
MAIN BOARD SHEET 8

POWER BOARD

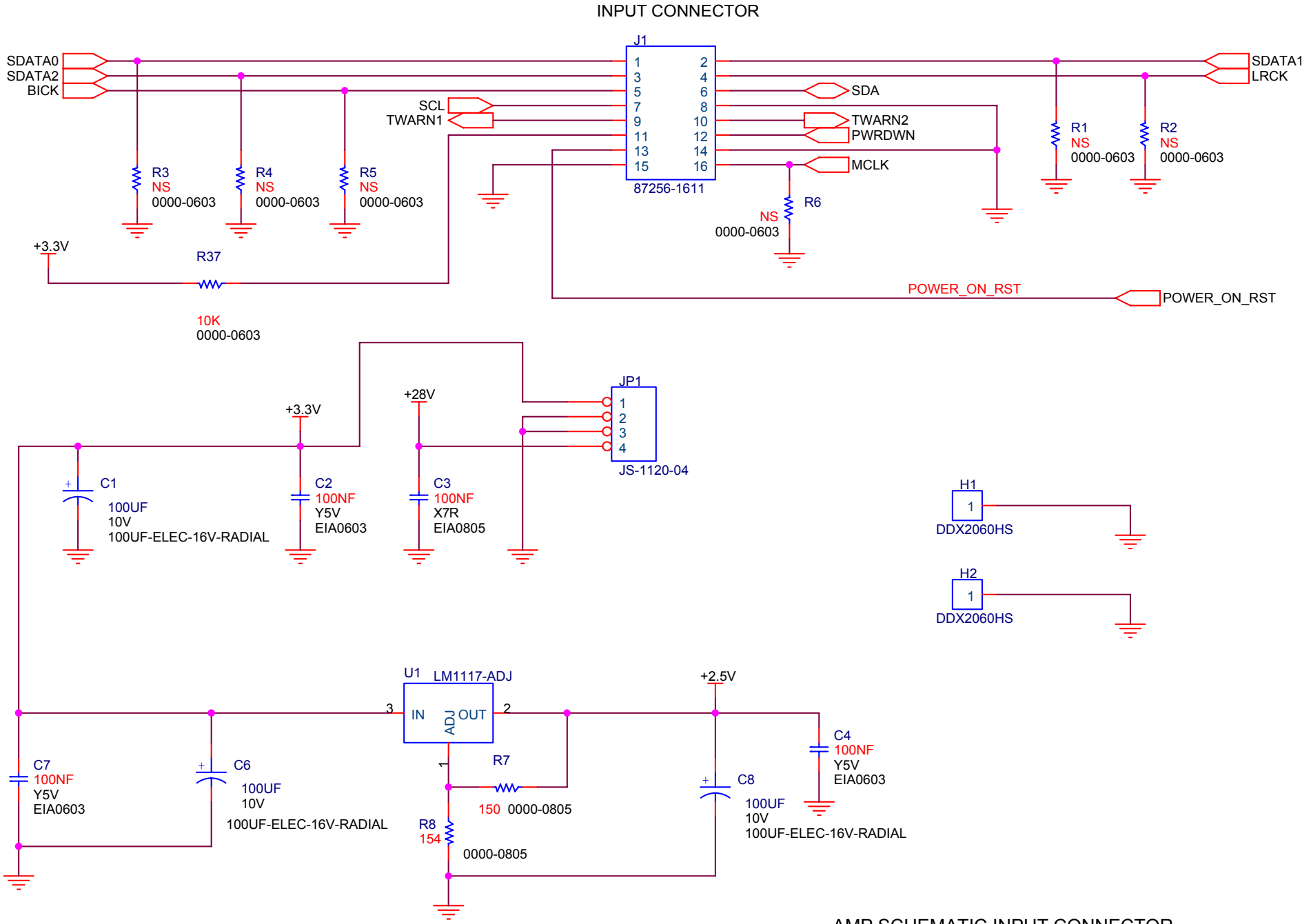

PL800
F800
3. 15A
L800
D805
GBU4M
C815
330u
400V
D801
1N4007
C854
1n
1kV
R803
4k7
TR800
SMPSAV1300 [LOW POWER 30027826]
+300
+30V
GND2
+8V
+15V
GND
-22V
NC1
NC4
DRAIN
NC3
NC2
VCC
GND1
F1
F2
n.c
IC800
MC44608
DEMAG
I_SENSE
CONT_IN
GND
VI
NC
VCC
DRIVER
JUMPER
4V7
Q801
MTP6N60E[PLASTIC]
W/US
IC803
TCET1106
IC804
TL431
Q810
BC848B
Q803
BC848B
IC807
MC34167
FEEDBACK
OUT
GND
VCC
STBY
IC805
LM7805
IC809
K47B812
IC806
LM317T
Q804
BC337
Q807
BC848B
Q806
BC848B
Q803
BC327
Q802
BC558B
Q805
BC848B
Q808
BC327
D809
BA159
D811
BYW29
D808
UF5402
D810
BYV28-200
D812
BA159
D817
1N4148
D814
BZX79C5V6
REFIN
SOGUTUCULU
+30V
+15VST
+12VST
+12V
+5V
+3V3
-22V
-5V
STBY
PL803
PL804
PL805
PL806
FL1
FL2

FRONT PANEL

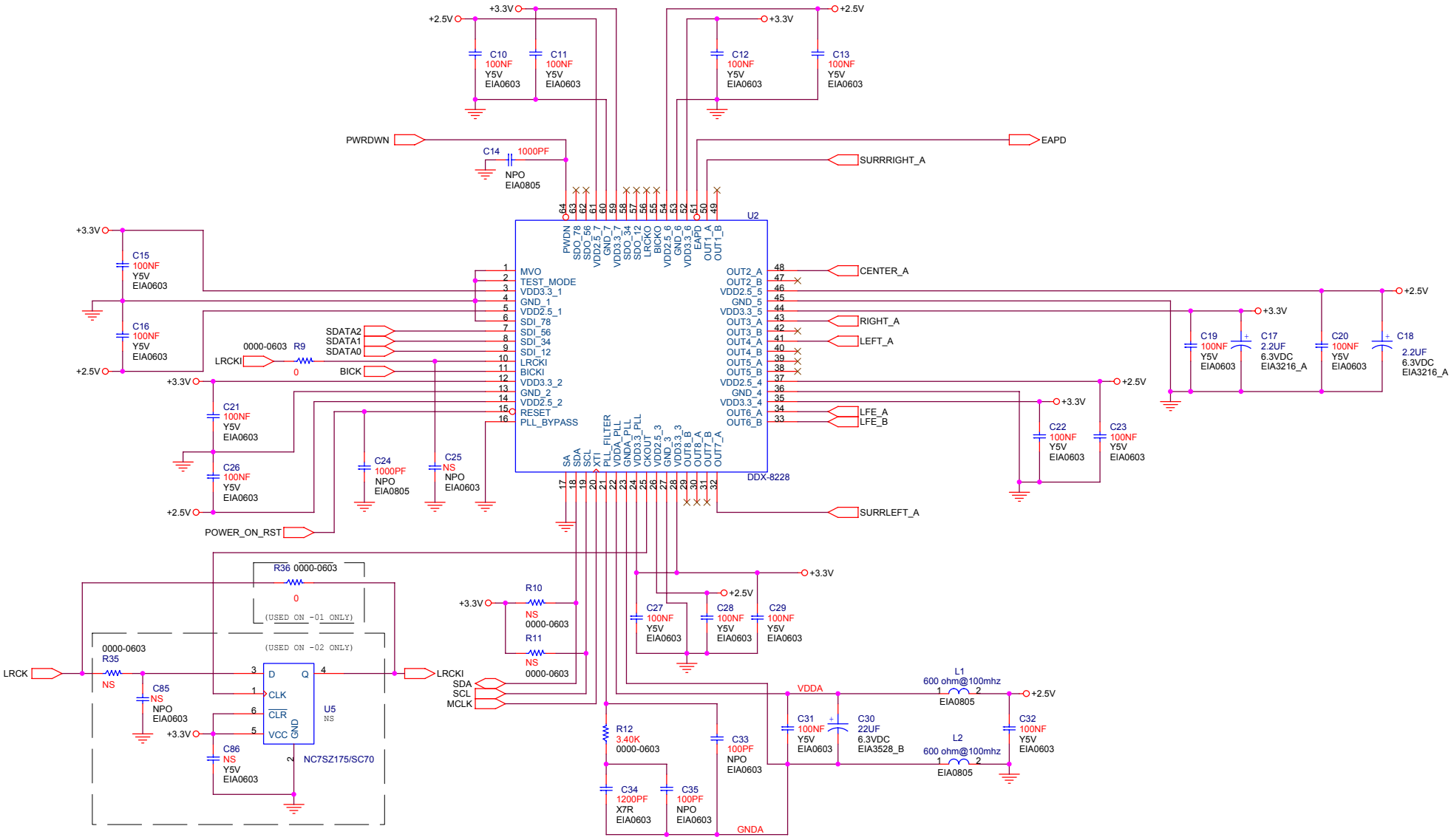

FRONT PANEL-I DATA CONNECTOR [DIGITAL BOARD]
PL101
R105 220R
R103 220R
R104 220R
R102 220R
VFD_DATA
VFD_CLK
VFD_CS
IR_IN
+5V
C103 50V 100n
C105
FRONT PANEL-I POWER CONNECTOR
PL102
FL1
FL2
-22V
C102 50V 100n
C106
MD1
DISPLAY_VFD_11_BT_234NK
IC101
PD16311
C103 C111
R109 220R
D1
STANDBY
R107 56K
C110 C108
IR_IN
TSOP1836
IC102
R123 4k7
R101 100R
C121 220p
C101
R110 2k2
R111 2k2
R112 2k2
C112 C119 C120 220p
R113 R114 R115 R116
R135 R136 R137
SW1 OPEN_CLOSE
SW2 PLAY_PAUSE
SW3 STOP
SW10 STANDBY/POWER
SW4 SEARCH_BACK
SW5 SEARCH FORWARD
SW6 SKIP BACK
SW7 SKIP FORWARD
SW8 VOLUME+
SW9 VOLUME-
SW11 MODE
D3 D4 D5 D6
1N4148
VFD_DATA
VFD_CLK
VFD_CS



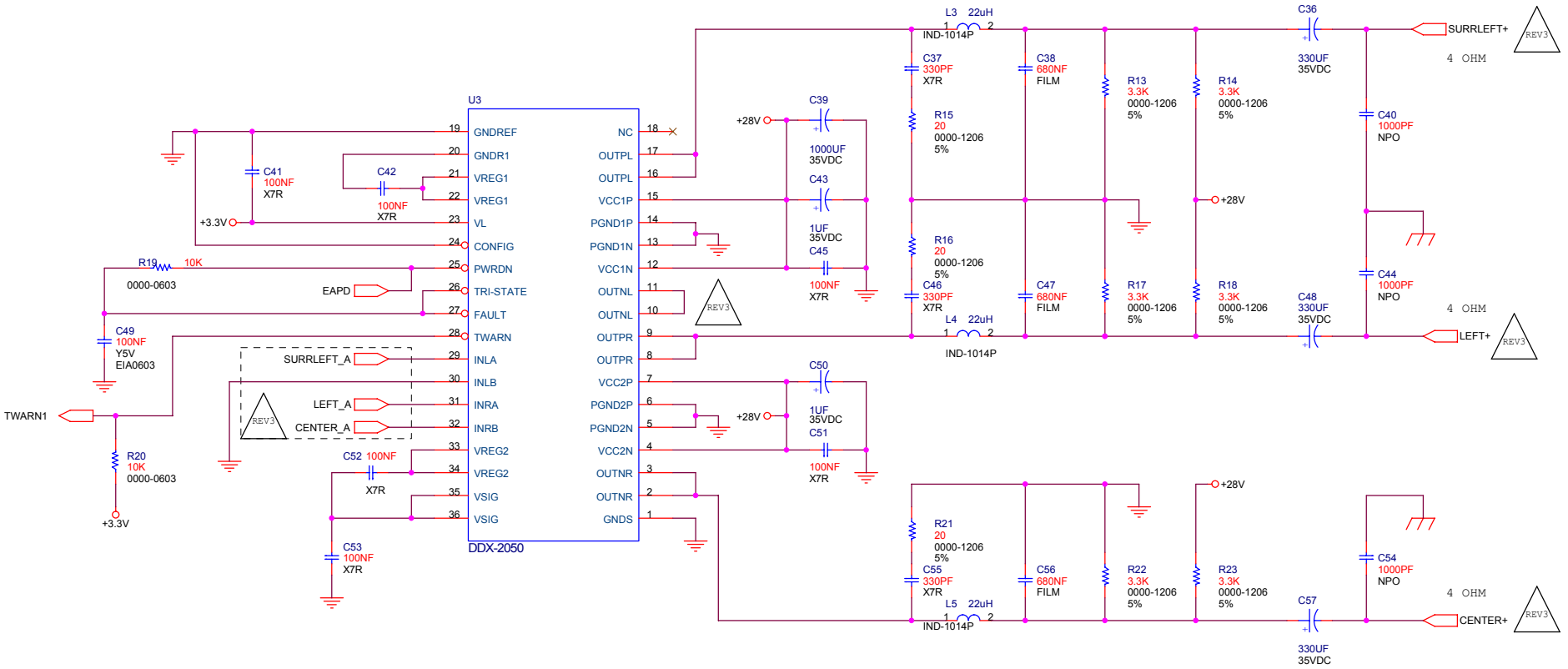
AMP SCHEMATICS 5X15W+1X25W



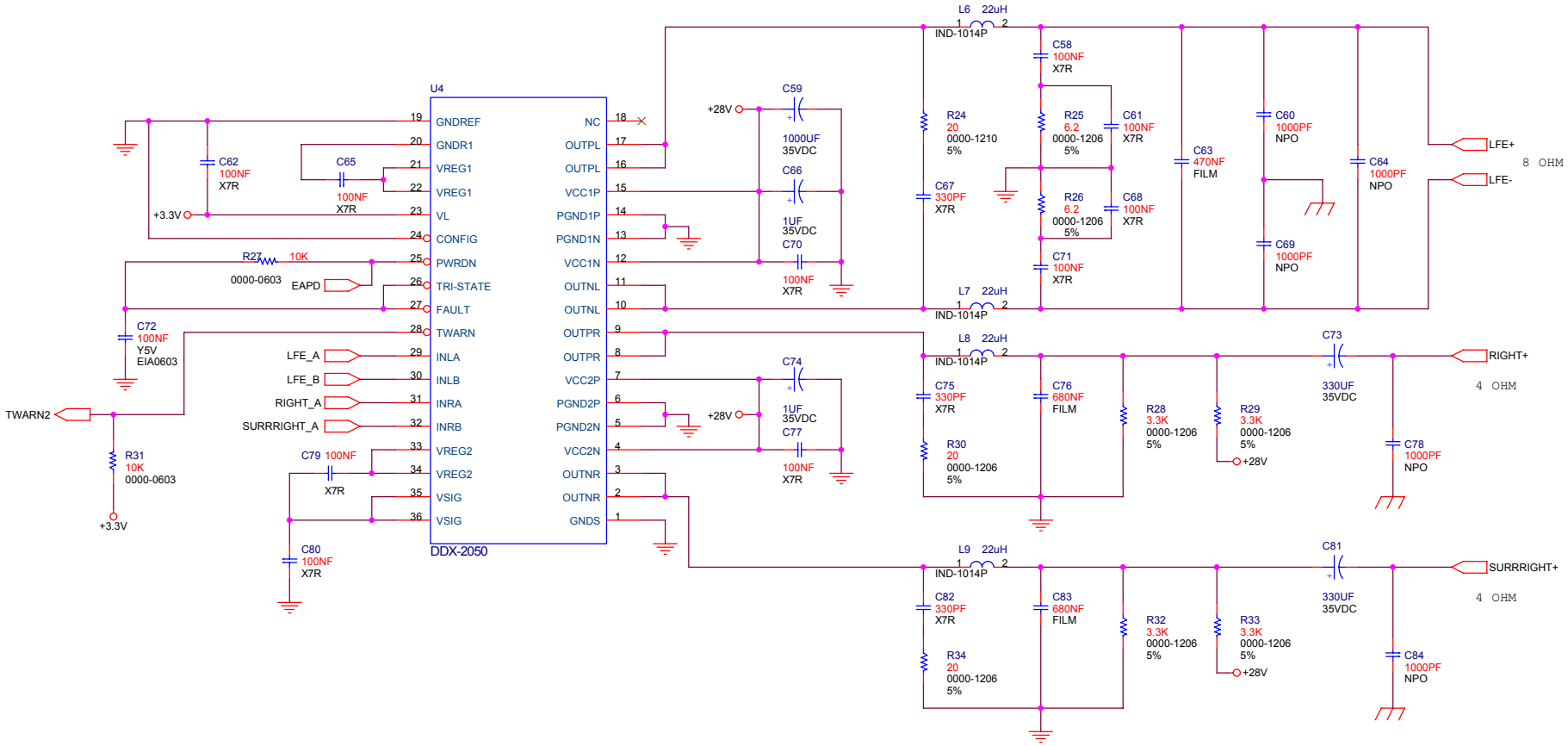
AMP SCHEMATIC INPUT CONNECTOR



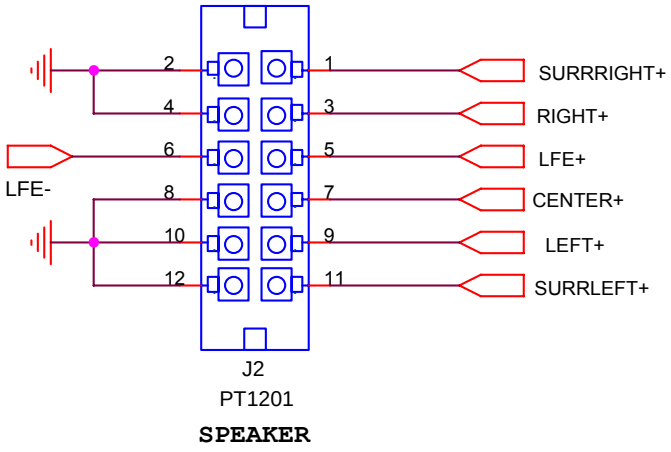
AMP SCHEMATIC PROCESSING

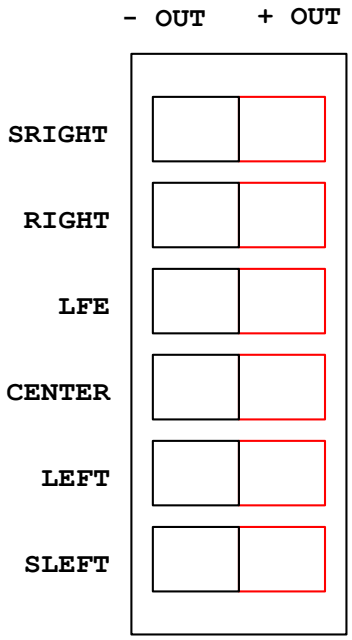


AMP SCHEMATIC LEFT, SURRLEFT CHANNELS AMPLIFIER



AMP SCHEMATIC CENTER, LFE CHANNEL AMPLIFIERS





Rear Panel View

AMP SCHEMATIC OUTPUT CONNECTOR

HITACHI

Hitachi, Ltd. Tokyo, Japan
International Sales Division
THE HITACHI ATAGO BUILDING,
No. 15 –12 Nishi Shinbashi, 2 – Chome,
Minato – Ku, Tokyo 105-8430, Japan.
Tel: 03 35022111

HITACHI EUROPE LTD,
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire
SL6 8YA
UNITED KINGDOM
Tel: 01628 643000
Fax: 01628 643400
Email: **consumer-service@hitachi-eu.com**

HITACHI EUROPE S.A.
364 Kifissias Ave. & 1, Delfon Str.
152 33 Chalandri
Athens
GREECE
Tel: 1-6837200
Fax: 1-6835964
Email: **service.hellas@hitachi-eu.com**

HITACHI EUROPE GmbH
Munich Office
Dornacher Strasse 3
D-85622 Feldkirchen bei München
GERMANY
Tel: +49-89-991 80-0
Fax: +49-89-991 80-224
Hotline: +49-180-551 25 51 (12ct/min)
Email: **HSE-DUS.service@hitachi-eu.com**

HITACHI EUROPE S.A.
Gran Via Carlos III, 86, planta 5
Edificios Trade - Torre Este
08028 Barcelona
SPAIN
Tel: +34 93 409 2550
Fax: +34 93 491 3513
Email: **atencion.cliente@hitachi-eu.com**

HITACHI EUROPE srl
Via Tommaso Gulli N.39, 20147
Milano, Italia
ITALY
Tel: +39 02 487861
Tel: +39 02 38073415 Servizio Clienti
Fax: +39 02 48786381/2
Email: customerservice.italy@hitachi-eu.com

HITACHI Europe AB
Box 77 S-164 94 Kista
SWEDEN
Tel: +46 (0) 8 562 711 00
Fax: +46 (0) 8 562 711 13
Email: **csgswe@hitachi-eu.com**

HITACHI EUROPE S.A.S
Lyon Office
B.P. 45, 69671 BRON CEDEX
FRANCE
Tel: +33 04 72 14 29 70
Fax: +33 04 72 14 29 99
Email: **france.consommateur@hitachi-eu.com**

HITACHI EUROPE LTD (Norway) AB
STRANDVEIEN 18
1366 Lysaker
NORWAY
Tel: 67 5190 30
Fax: 67 5190 32
Email: **csgnor@hitachi-eu.com**

HITACH EUROPE AB
Egebækgård
Egebækvej 98
DK-2850 Nærum
DENMARK
Tel: +45 43 43 6050
Fax: +45 43 60 51
Email: **csgnor@hitachi-eu.com**

HITACHI EUROPE AB
Neopoli / Niemenkatu 73
FIN-15140 Lahti
FINLAND
Tel : +358 3 8858 271
Fax: +358 3 8858 272
Email: **csgnor@hitachi-eu.com**

Hitachi Europe Ltd
Bergensesteenweg 421
1600 Sint-Pieters-Leeuw
BELGIUM
Tel: +32 2 363 99 01
Fax: +32 2 363 99 00
Email: **sofie.van.bom@hitachi-eu.com**

HITACHI EUROPE LTD
Na Sychrove 975/8
101 27 Praha 10 – Bohdalec
CZECH REPUBLIC
Tel: +420 267 212 383
Fax: +420 267 212 385
Email: **csgnor@hitachi-eu.com**

www.hitachidigitalmedia.com